SuperH SolutionEngine

Super I/O Daughter Board

(MSSIODB01E)

User's Manual

1st Edition

Hitachi ULSI Systems Co., Ltd

MSSIODB01E-M

Cautions

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Notes on Using the Super I/O Daughter Board

This section contains topics to be carefully read and considered when using the SuperI/O daughter board (hereafter the MSSIODB01) of the Hitachi LSI systems.

(Components of the MSSIODB01)

1. After opening the package, check the following items to confirm that everything is in place.

a. Super I/O daughter board

b. Super I/O daughter board user's manual (this manual)

(How to connect the SolutionEngine)

2. Before connecting SuperH SolutionEngine(hereafter SolutionEngine), the power must be turned off.

(Installation)

3. The MSSIODB01 is developed for evaluation of products before they are put under the development phase. Do not incorporate the MSSIODB01 into any of the products.
4. Do not install the MSSIODB01 in an area subject to direct sunlight and other areas exposed to heaters or other source of high temperatures.
5. Do not choose area subject to extremely dusty condition.
6. Use care to keep the board free from contact with pieces of wire, soldering waste and other foreign matter.

1. Features

The MSSIODB01 is the daughterboard connectable to the SolutionEngine. The MSSIODB01 has the SMSC-supplied super I/O (FDC37C935), the EPSON-supplied LCD controller (SED1354) and infrared remote control receive microcomputer (HD4074344) for home use(NEC format). The MSSIODB01 is capable of evaluating various I/O.

1.1. Features of the MSSIODB01

The MSSIODB01 has the following features.

1. The MSSIODB01 can be connected to the SolutionEngine directly.
2. The MSSIODB01 can connect the SolutionEngine and various devices. The following devices can be connected to the SolutionEngine.
   a. PS/2 interface 2ch is equipped and keyboard and mouse can be connected.
   b. The MSSIODB01 receive code of infrared remote control for home use, and can send the received code to SH.
   c. RS232C interface output 1ch is equipped, and modem and other equipments can be connected
   d. IDE interface 1ch is equipped and HDD, CD-ROM can be connected.
   e. VGA-capable LCD controller (EPSON-supplied SED1354) is equipped and LCD can be connected.

1.2. System Configuration

Figure1.1 shows the MSSIODB01 system configuration, and figure 1.2 shows the external view of the MSSIODB01. Prepare various devices such as mouse, keyboard and modem to be connected to the MSSIODB01.

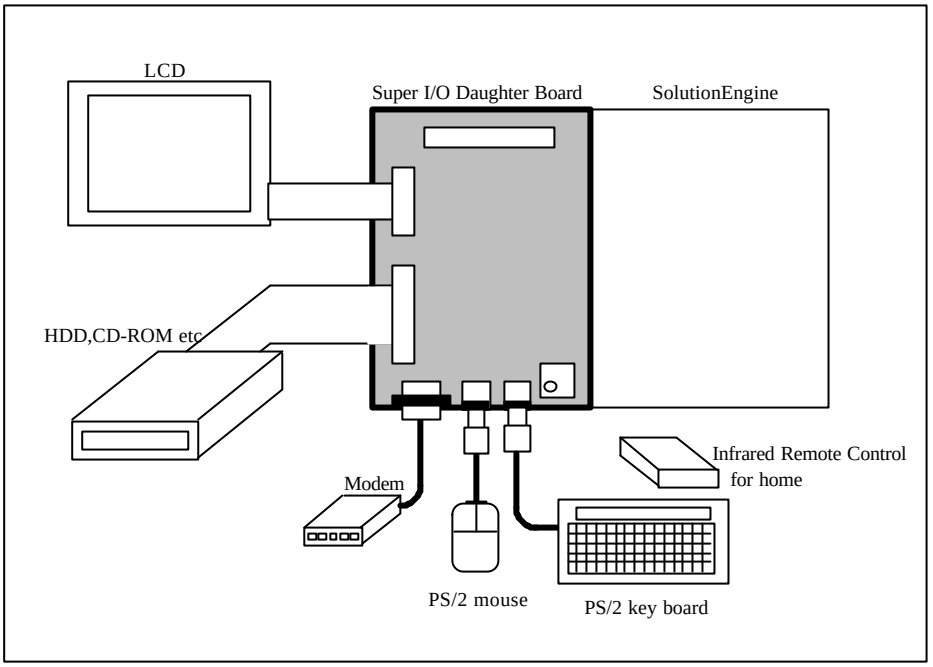


Figure1.1 Configuration of the Super I/O Daughter Board

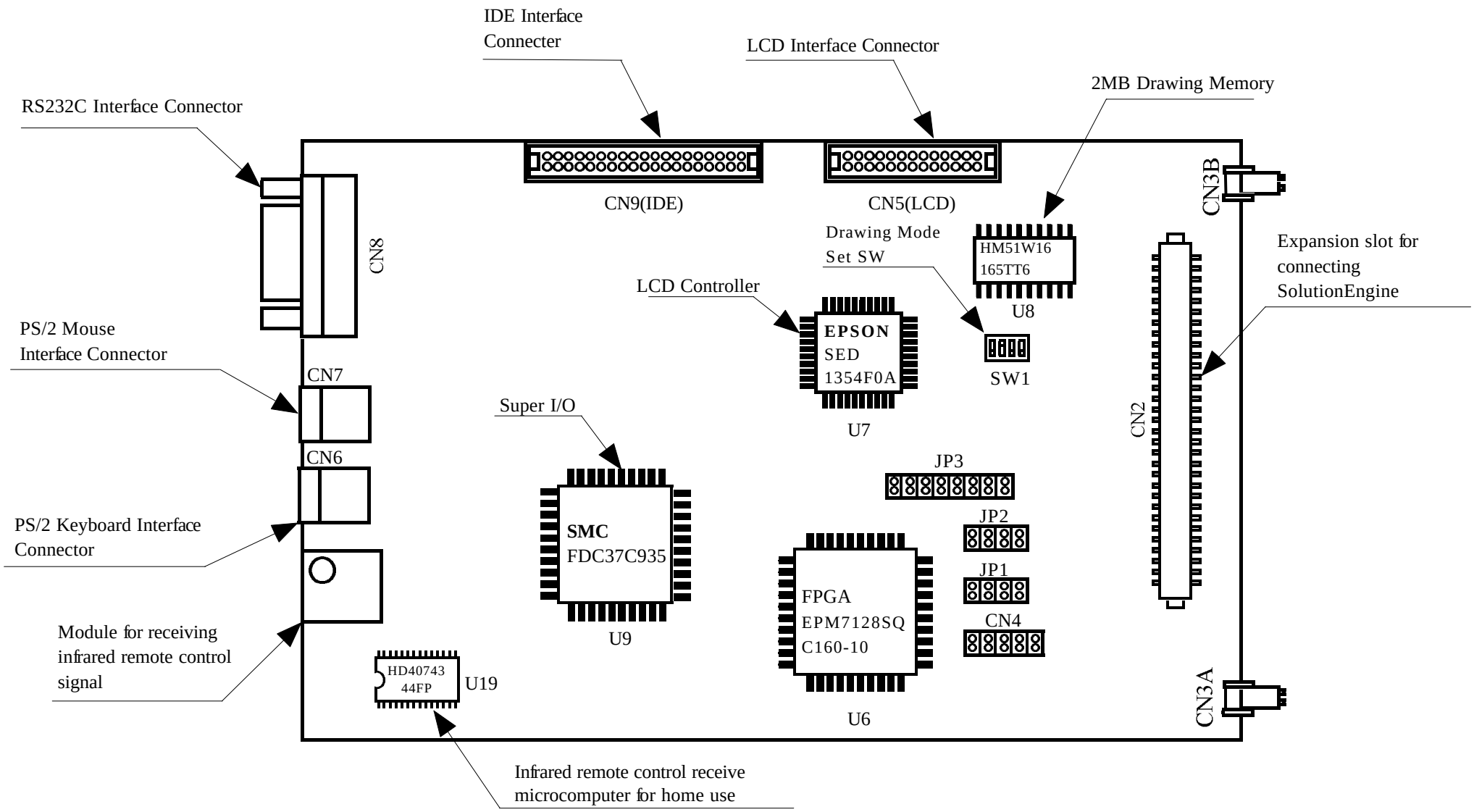


Figure1.2 External View of Super I/O Daughter Board

2. Specification

2.1. System Specification

Table2.1 lists the specification of the MSSIODB01 function.

Table2.2 lists the power supply and the environmental factors.

Table2.1 MSSIODB01 Specifications

Function	Specification
Device	Super I/O : FDC37C935 (SMSC) LCD Controller: SED1354F (EPSON) LCD Display Memory: HM51W16165 (Hitachi-supplied DRAM 1Mx16-bit) Remote Control Receive: HD4074344 (Hitachi-supplied 4-bit microcomputer)
PS/2 Interface	Mouse x1ch, Keyboard x1ch
Serial Interface	RS232C x1ch
IDE Interface	40-pin connector x1
Infrared Remote Control Receive	1ch (NEC format)
Resolution of LCD	320 x240, 480 x320 , 640 x240 , 640 x480 , 800 x600
Displayed Color of LCD	Monochrome LCD: 16 level Passive color LCD: Maximum 4096 colors Active Matrix TFT LCD: Maximum 65536 colors
CPU interface	3.3V (can be connected directly to expansion slot of the SolutionEngine)
Interrupt	IRQ1, IRQ3, IRQ4, IRQ5, IRQ6 are used
DMA	Ch0 ,Ch1 are selectable
WAIT output	WAIT0-WAIT3 are selectable

Table2.2 MSSIODB01 Power Supply , Dimensions and Environmental Factors

Item	Specification
Environment	Operation Condition -Temperature: 10-35 degree C -Humidity: 30-85%RH(no condensation) -Ambient gas: Should not have corrosive gas
Operation Voltage	3.3V, 5V (Supplied from the expansion slot of the SolutionEngine)
Consumption Current	500mA (only board)
External Dimension	B6 size (128mm x 182mm)

2.2. Block Diagram

Figure2.2 shows the MSSIODB01 block diagram.

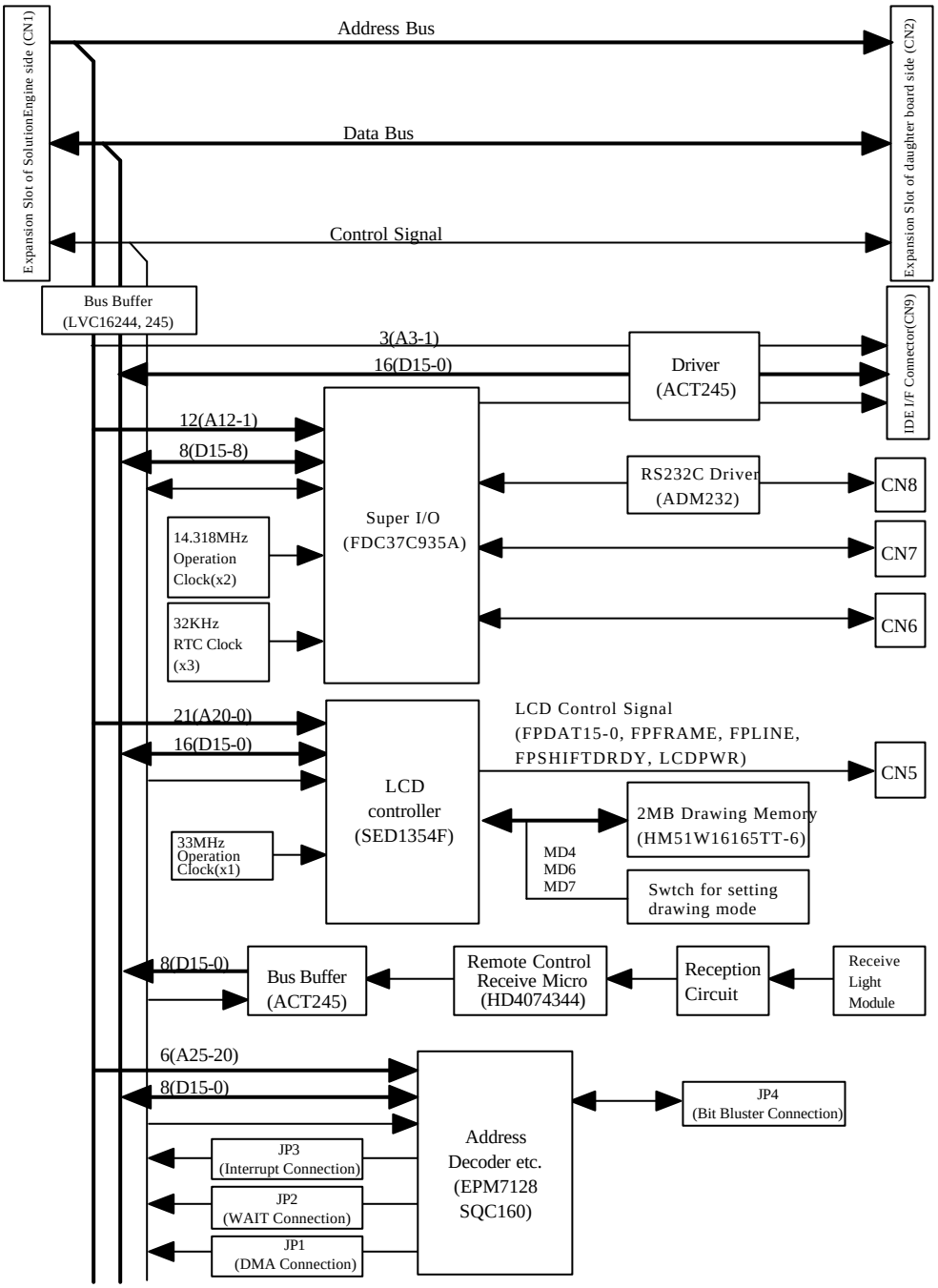


Figure2.1 Block Diagram of MSSIODB01

3. Switch and Jumper Pin Functions

3.1. LCD Controller Drawing Mode Setting Switch (SW1)

Figure3.1 shows the function of DIP switch that set various operation mode of the LCD controller.

Table 3.1 lists the DIP switch functions.

As listed in table3.1, SW1 can select the size of drawing memory and endian.

Set the same endian as the SolutionEngine.

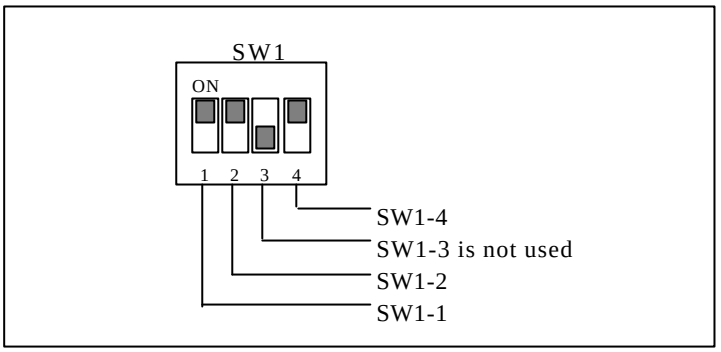


Figure3.1 LCD Controller Drawing Mode Setting Switch

Table3.1 Function of LCD Controller Drawing Mode Setting Switch

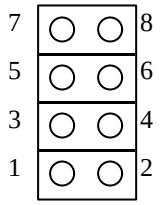
SW	Name	Function
SW1-1 SW1-2	Select external memory	SW1-1 and SW1-2 are connected to MD7 and MD6 of SED1354F0A and selects external memory. [SW1-1: OFF, SW1-2: OFF] Symmetrical 256K x16 DRAM [SW1-1: OFF, SW1-2: ON] Symmetrical 1M x16 DRAM [SW1-1: ON, SW1-2: OFF] Asymmetrical 256K x16 DRAM [SW1-1: ON, SW1-2: ON](at shipment) Asymmetrical 1M x16 DRAM
SW1-3	Not used	Not connected
SW1-4	Select endian	SW1-4 is connected to MD4 of SED1354F0A and selects endian. [ON] (at shipment) Little endian [OFF] Big endian

3.2. DMA Connection (JP1)

Table 3.2 lists the function of DMA connection (JP1). As listed in table3.2, DMAREQ and DMAACK of the daughter board are connected to DREQn and DACKn of CPU on the SolutionEngine.

When DMA is not used, make JP1 open.

Table3.2 Function of DMA connection



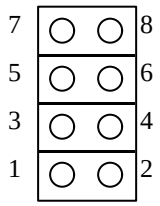
JP1
(DMA)

Pin No.	Function
JP1-1, JP1-2	By making this pin closed, DMAACK set at DMA connection setting register in FPGA is connected to DACK0 of CPU.
JP1-3, JP1-4	By making this pin closed, DMAREQ set at DMA connection setting register in FPGA is connected to DREQ0 of CPU.
JP1-5, JP1-6	By making this pin closed, DMAACK set at DMA connection setting register in FPGA is connected to DACK1 of CPU.
JP1-7, JP1-8	By making this pin closed, DMAREQ set at DMA connection setting register in FPGA is connected to DREQ1 of CPU.

3.3. WAIT Connection (JP2)

Table3.3 lists function of WAIT connection (JP2). As listed in table3.3, by making jumper pin closed, WAIT signal is connected to any of WAIT0-3 of the SolutionEngine. Be sure to make any pin closed.

Table3.3 Function of WAIT connection



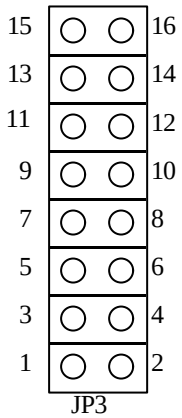
JP2
(WAIT)

Pin No.	Function
JP2-1, JP2-2	By making this pin closed, WAIT signal in daughter board is connected to WAIT0 of the SolutionEngine.(at shipment)
JP2-3, JP2-4	By making this pin closed, WAIT signal in daughter board is connected to WAIT1 of the SolutionEngine.
JP2-5, JP2-6	By making this pin closed, WAIT signal in daughter board is connected to WAIT2 of the SolutionEngine.
JP2-7, JP2-8	By making this pin closed, WAIT signal in daughter board is connected to WAIT3 of the SolutionEngine.

3.4. Interrupt Connection (JP3)

Table3.4 lists function of interrupt connection (JP3). As listed in table3.4, by making jumper pin closed, interrupt signal is connected to any of IRQ1, IRQ3-IRQ6 of the SolutionEngine.

Table3.4 Function of interrupt connection(JP3)



JP3
(IRQ)

Pin No.	Function
JP3-1, JP3-2	By making this pin closed, keyboard interrupt signal is connected to IRQ1 of the SolutionEngine.
JP3-3, JP3-4	Not used (Be sure to make open)
JP3-5, JP3-6	By making this pin closed, serial port interrupt signal is connected to IRQ3 of the SolutionEngine.
JP3-7, JP3-8	By making this pin closed, mouse interrupt signal is connected to IRQ4 of the SolutionEngine.
JP3-9, JP3-10	By making this pin closed, IDE interrupt signal is connected to IRQ5 of the SolutionEngine.
JP3-11, JP3-12	By making this pin closed, infrared interrupt signal is connected to IRQ6 of the SolutionEngine.
JP3-13, JP3-14	Not used (Be sure to make open)
JP3-15, JP3-16	Not used (Be sure to make open)

4. LED Functions

4.1. Power LED (D1)

This LED indicates that 5V power is correctly turned on. Functions are as follows.

LED ON: 5V power is supplied to the daughter board.

LED OFF: 5V power is not supplied to the daughter board.

4.2. Power LED (D2)

This LED indicates that 3.3V power is correctly turned on. Functions are as follows.

LED ON: 3.3V power is supplied to the daughter board.

LED OFF: 3.3V power is supplied to the daughter board.

4.3. RESET LED (D3)

This LED indicates that Reset is in effect. Functions are as follows.

LED ON: Reset is in effect

LED OFF: RESET is cleared

4.4. IDE LED (D3)

This LED indicates that IDE is accessed.

LED ON: IDE is accessed.

LED OFF: IDE is not accessed.

5. Memory Map

Figure5.1 shows the memory map of the MSSIODB01. As shown in figure 5.1, various kinds of peripheral LSI on the MSSIODB01 is placed at area2 and area4 on the SolutionEngine.

Figure5.1 Memory map of the MSSIODB01

Area	Space Name	Bus Width	Space	Device	Remarks
Area2	Expansion Area2	16-Bit 2WAIT	2MB h’08000000 -h’081FFFFF	LCD Controller SED1354 Control Register (EPSON)	
			2MB h’08200000 -h’083FFFFF	Drawing Memory HM51W16165TT-6 (Hitachi)	
			60MB h’08400000 -h’0BFFFFFF	Expansion Area	
Area4	16-Bit Peripheral Device Control Register area	16-Bit 2WAIT	1MB h’12000000 -h’120FFFFF	Super I/O FDC37C935A (SMSC)	IDE(8-bit) PS/2 keyboard PS/2 mouse serial
			1MB h’12100000 -h’121FFFFF	IDE (Data Bus Width 16-Bit)	
			1MB h’12200000 -h’122FFFFF	Infrared Remote Control HD4074344 (Hitachi)	Infrared Remote Control Receive Data Register
			1MB h’12300000 -h’123FFFFF	System Control Register in FPGA	

6. Function Blocks

6.1. LCD Controller Control Block

1. Register Map

Table6.1 lists the register map of LCD controller SED1354. As listed in table6.1, internal register of LCD controller SED1354 is placed from the first of area2.

Each register can be accessed in byte, word and longword size. When accessing in word and longword size, access 2n address and 4n address.

When MMU is not used, a is input to *.

When MMU is used, 0 is input to *.

Table6.1 Register map of LCD Controller SED1354

Address	SED1354 Register	Function	Address	SED1354 Register	Function
h'*8000000	REG[00h]	Revised Code Register	h'*8000016	REG[16h]	Memory Address Offset Set Register0
h'*8000001	REG[01h]	Memory Configuration Register	h'*8000017	REG[17h]	Memory Address Offset Set Register1
h'*8000002	REG[02h]	Panel Type Set Register	h'*8000018	REG[18h]	Pixel Panning Register
h'*8000003	REG[03h]	MOD rate Set Register	h'*8000019	REG[19h]	Clock Set Register
h'*8000004	REG[04h]	Horizontal Display Size Set Register	h'*800001a	REG[1ah]	Power Save Set Register
h'*8000005	REG[05h]	Horizontal Not display Time Set Register	h'*800001b	REG[1bh]	Disable Register
h'*8000006	REG[06h]	HRTC/FPLINE Start Place Set Register	h'*800001c	REG[1ch]	MD Set Read Back Register0
h'*8000007	REG[07h]	HRTC/FPLINE Pulse Width Set Register	h'*800001d	REG[1dh]	MD Set Read Back Register1
h'*8000008	REG[08h]	Vertical Display Size Set Register0	h'*800001e	REG[1eh]	GPIO Set Register0
h'*8000009	REG[09h]	Vertical Display Size Set Register1	h'*800001f	REG[1fh]	GPIO Set Register1
h'*800000a	REG[0ah]	Vertical Non-display Time Set Register	h'*8000020	REG[20h]	GPIO Status/Control Register0
h'*800000b	REG[0bh]	VRTC/FPFRAME Start Place Set Register	h'*8000021	REG[21h]	GPIO Status/Control Register1
h'*800000c	REG[0ch]	VRTC/FPFRAME Pulse Width Set Register	h'*8000022	REG[22h]	Performance Improvement Register0
h'*800000d	REG[0dh]	Display Mode Register	h'*8000023	REG[23h]	Performance Improvement Register1
h'*800000e	REG[0eh]	Screen 1line Set Register0	h'*8000024	REG[24h]	Lookup Table Address Register
h'*800000f	REG[0fh]	Screen 1line Set Register1	h'*8000025	REG[25h]	Unused
h'*8000010	REG[10h]	Screen 1 Display Start Address Set Register0	h'*8000026	REG[26h]	Lookup Table Data Register
h'*8000011	REG[11h]	Screen 1 Display Start Address Set Register1	h'*8000027	REG[27h]	Lookup Table Bank Select Register
h'*8000012	REG[12h]	Screen 1 Display Start Address Set Register2	h'*8000028 h'*8000029	REG[28h] REG[29h]	RAMDAC Pixel Read Mask Register
h'*8000013	REG[13h]	Screen 2 Display Start Address Set Register0	h'*800002a h'*800002b	REG[2ah] REG[2bh]	RAMDAC Read Mode Address Register
h'*8000014	REG[14h]	Screen 2 Display Start Address Set Register1	h'*800002c h'*800002d	REG[2ch] REG[2dh]	RAMDAC Write Mode Address Register
h'*8000015	REG[15h]	Screen 2 Display Start Address Set Register2	h'*800002e h'*800002f	REG[2eh] REG[2fh]	RAMDAC Pallet Data Register

2. Drawing Memory Configuration

Table6.2 lists relation between memory/display and level/display color.

Table6.2 Relation between level/display color and memory/display

Level, Display Color	Memory Configuration	Panel Display
1-bit/pixel	b7 … b0 A0 A1 A2 A3 A4 A5 A6 A7	P0 P1 P2 P3 P4 P5 P6 P7 Pn = An
2-bit/pixel	b7 … b0 A0 B0 A1 B1 A2 B2 A3 B3 A4 B4 A5 B5 A6 B6 A7 B7	P0 P1 P2 P3 P4 P5 P6 P7 Pn = (An,Bn)
4-bit/pixel	b7 … b0 A0 B0 C0 D0 A1 B1 C1 D1 A2 B2 C2 D2 A3 B3 C3 D3 A4 B4 C4 D4 A5 B5 C5 D5	P0 P1 P2 P3 P4 P5 P6 P7 Pn = (An,Bn,Cn,Dn)
8-bit/pixel	b7 … b0 $R0^2$ $R0^1$ $R0^0$ $G0^2$ $G0^1$ $G0^0$ $B0^1$ $B0^0$ $R1^2$ $R1^1$ $R1^0$ $G1^2$ $G1^1$ $G1^0$ $B1^1$ $B1^0$ $R2^2$ $R2^1$ $R2^0$ $G2^2$ $G2^1$ $G2^0$ $B2^1$ $B2^0$	P0 P1 P2 P3 P4 P5 P6 P7 $Pn = (Rn^{2-0}, Gn^{2-0}, Bn^{1-0})$
15-bit/pixel	b7 … b0 $G0^2$ $G0^1$ $G0^0$ $B0^4$ $B0^3$ $B0^2$ $B0^1$ $B0^0$ $R0^4$ $R0^3$ $R0^2$ $R0^1$ $R0^0$ $G0^4$ $G0^3$ $G1^2$ $G1^1$ $G1^0$ $B1^4$ $B1^3$ $B1^2$ $B1^1$ $B1^0$ $R1^4$ $R1^3$ $R1^2$ $R1^1$ $R1^0$ $G1^4$ $G1^3$	P0 P1 P2 P3 P4 P5 P6 P7 TFT $Pn = (Rn^{4-0}, Gn^{4-0}, Bn^{4-0})$ Passive $Pn = (Rn^{4-1}, Gn^{4-1}, Bn^{4-1})$
16-bit/pixel	b7 … b0 $G0^2$ $G0^1$ $G0^0$ $B0^4$ $B0^3$ $B0^2$ $B0^1$ $B0^0$ $R0^4$ $R0^3$ $R0^2$ $R0^1$ $R0^0$ $G0^5$ $G0^4$ $G0^3$ $G1^2$ $G1^1$ $G1^0$ $B1^4$ $B1^3$ $B1^2$ $B1^1$ $B1^0$ $R1^4$ $R1^3$ $R1^2$ $R1^1$ $R1^0$ $G1^5$ $G1^4$ $G1^3$	P0 P1 P2 P3 P4 P5 P6 P7 TFT $Pn = (Rn^{4-0}, Gn^{5-0}, Bn^{4-0})$ Passive $Pn = (Rn^{4-1}, Gn^{5-2}, Bn^{4-1})$

3. Register Setting

Figure6.1 shows the method to set the register of LCD controller SED1354. As figure6.1 shows, be sure to set the bus controller of SH microcomputer, set power save setting register (h'800001a) of SED1354 and set disable register (h'800001b) before accessing various kinds of register and drawing memory. To access each register and drawing memory, be sure to set bit7 of disable register to 0.

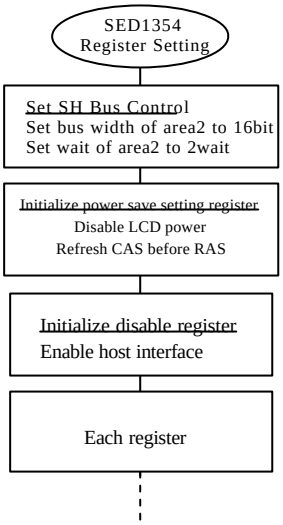
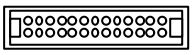


Figure6.1 Method to set SED1354 register

4. LCD Interface Connector(CN5)

Figure6.2 shows the pin assignment of the LCD interface connector. As shown in figure 6.2, various signals for display is output from the LCD interface connector.

Connector: PS-30PE-D4T1-B1
(JAE)



Pin No.	Signal	Function	Pin No.	Signal	Function
1	FPDAT15	Panel Display Data D15-D0	17	GND	Ground
2	FPDAT14		18	GND	Ground
3	FPDAT13		19	FPSHIFT	Line Pulse
4	FPDAT12		20	GND	Ground
5	FPDAT11		21	DRDY	TFT: Display Enable Passive: 2nd shift clock
6	FPDAT10				
7	FPDAT9		22	GND	Ground
8	FPDAT8		23	LCDPWR	LCD power control output
9	FPDAT7		24	GND	Ground
10	FPDAT6		25	FPLINE	Line Pulse
11	FPDAT5		26	GND	Ground
12	FPDAT4		27	FPFRAME	Flame Pulse
13	FPDAT3		28	GND	Ground
14	FPDAT2		29	GND	Ground
15	FPDAT1		30	GND	Ground
16	FPDAT0				

Figure6.2 Pin assignment of LCD interface connector(CN5)

6.2. Super I/O Control Block

1. Register Map

Table6.3 lists the memory map of the super I/O configuration port. Super I/O FDC37C935A can set interrupt used by the serial controller via the configuration port. SYSOPT pin is pulled up to 10K-ohm and the configuration port address is h'370. When MMU is not used, b is input to *. When MMU is used, 1 is input to *.

Table6.3 Register Map

Address	Super I/O Address	Register Name
h'*20006e0	h'370	CONFIG PORT
h'*20006e0	h'370	INDEX PORT
h'*20006e2	h'371	DATA PORT

2. Register Access Method

Super I/O address bus (A11-A0) is connected to SH address bus (A12-A1). To access h'370 configuration port from SH, access to the address calculated from following equation.

SH Access Address=Offset (h'*2000000)+Super I/O Address x

(Example) configuration port address

SH access address=h'*2000000+h'370 x2

=h'*20006e0

Area4 where super I/O is placed is 16-bit bus width. So access register in 16-bit bus width. When accessing in 16-bit bus width, higher-order 8-bit become valid.

3. Initializing

Figure6.3 shows the serial initializing flow. As shown in figure6.3, initialize internal register (LCR,DLL,DLM etc.) of serial after initializing configuration.

Initializing configuration initializes base address to h ‘3f8. So start address of internal register is h’*2007f0(h’3f8 x2+h*2000000(start address of area4)).

For details, refer to the SMSC-supplied manual.

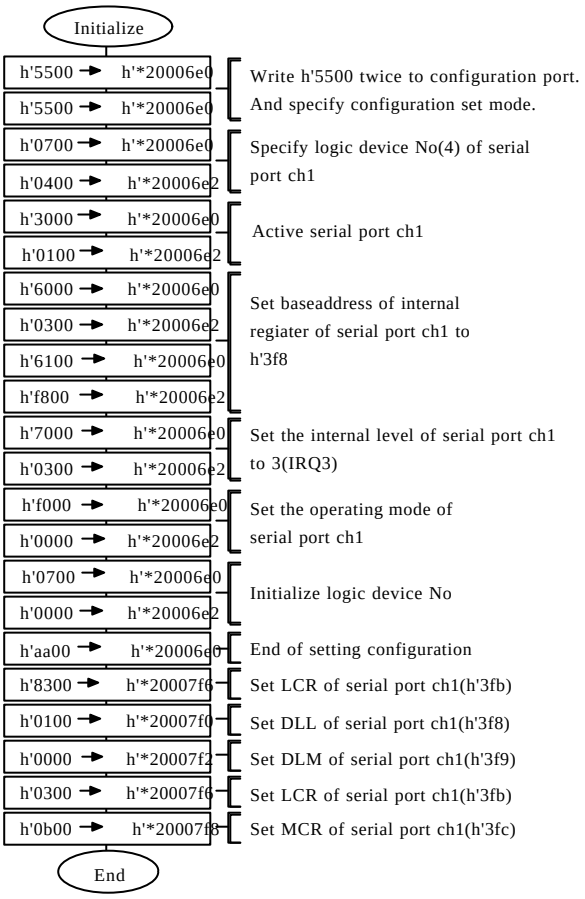


Figure6.3 Initializing flow of serial ch1

4. Pin assignment of CN6-8

Figure6.4 shows pin assignment of connector CN6-8 of super I/O peripheral.

Connector: MD-S6100-90
(NICHIATSU)

Pin Assignment of CN6

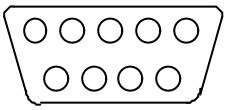
Pin No.	Signal
1	DATA
2	NC
3	GND
4	+5V
5	CLOCK
6	NC

Connector: MD-S6100-90
(NICHIATSU)

Pin Assignment of CN7

Pin No.	Signal
1	DATA
2	NC
3	GND
4	+5V
5	CLOCK
6	NC

Connector: DELC-J9PAF-23L6
(JAE)



Pin Assignment of CN8

Pin No.	Signal	Pin No.	Signal
1	DCD	6	DSR
2	RXD	7	RTS
3	TXD	8	CTS
4	DTR	9	RI
5	GND		

Figure6.4 Pin assignment of CN6 to CN8

6.3. IDE Control Block

1. Block Diagram

Figure6.5 shows the block diagram of IDE control block. As shown in figure6.5, super I/O and FPGA register control IDE.

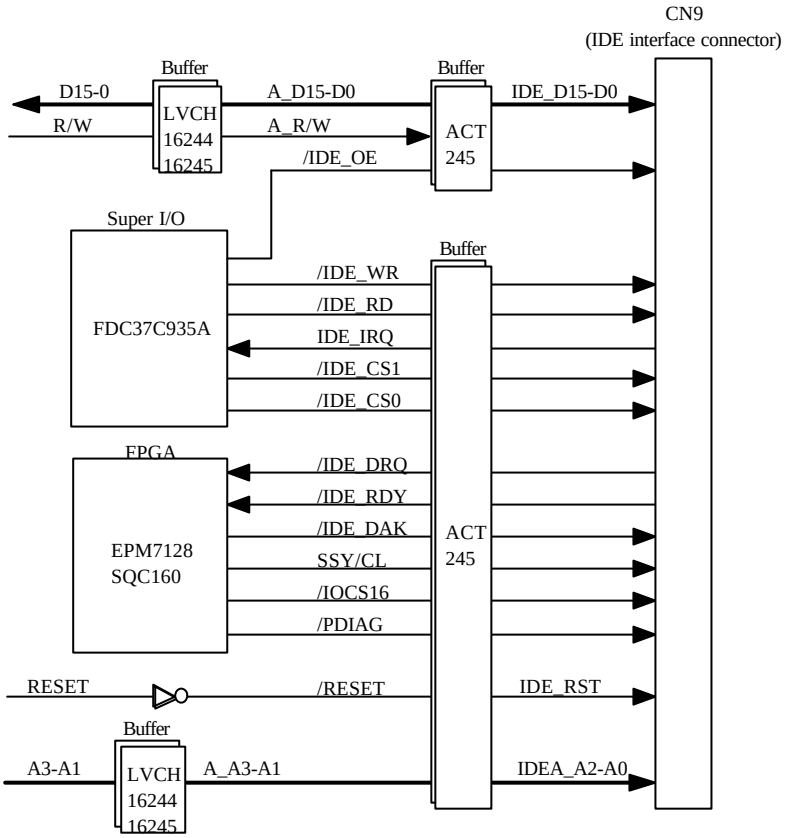


Figure6.5 Block diagram of IDE control block

2. Register Map

Table6.4 lists the register map of IDE control block. When the MMU is not used ,b is input to *. When the MMU is used , 1 is input to *.

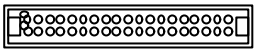
Table6.4 IDE Control Block Register Map

Address	Connected register	Function
h'*20003e0-h'*20003ee	Super I/O internal register (h'1f0-h'1f7) (h'3f6)	TASK FILE register
h'*20007ec		MISC.AT register
h'*2100000-h'*21fffff	IDE connecting register	Allocate internal register of various device connected to IDE
h'*2300001	Register that control FPGA	IDE Set Register
h'*2300002		DMA Connection Set Register

3. IDE Interface Connector (CN9)

Figure6.6 shows the pin assignment of IDE interface connector (CN9).

Connector: PS-40PE-D4T1-B1



Pin No.	Signal	Pin No.	Signal
1	IDE Reset	21	IDE DMA Request
2	GND	22	GND
3	D7	23	IDE WR
4	D8	24	GND
5	D6	25	IDE RD
6	D9	26	GND
7	D5	27	IDE RDY
8	D10	28	SSYNC/CSEL
9	D4	29	IDE DACK
10	D11	30	GND
11	D3	31	IDE IRQ
12	D12	32	IOCS16
13	D2	33	IDE A1
14	D13	34	PDIAG
15	D1	35	IDE A0
16	D14	36	IDE A2
17	D0	37	IDE CS0
18	D15	38	IDE CS1
19	GND	39	DASP
20	NC	40	GND

Figure6.6 Pin assignment of IDE interface connector(CN9)

6.4. FPGA Control Register

1. IDE Set Register (h'b2300001, h'12300001)

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	0	PDIAG/CSEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

-Initial value: h'00

-D15-D9: The write value should always be 0. 0 These bits always read 0.

-D8:

On reading: Signal to inform device 0 that diagnose of device 1 is completed.

0: enable

On writing: 0 is recognized as device 0 and 1 is recognized as device1.

2. DMA Connection Set Register (h'b2300002, h'12300002)

D15	D14	D13	D12	D11	D10	D9	D8
0	MSK1	MSK0	CHG	SET3	SET2	SET1	SET0
W	W	W	W	W	W	W	W

-Initial value: h'00

-D15: The write value should always be 0.

-D14,D13: Signal to mask DMA. MSK1 mask DMA1 and MSK 0 mask DMA0.

-D12: Following setting is reversed by 1.

-D11-D8: Connect DMA controller and each DMA.

Set Value (SET3-0)	Connection
0000	CPU_DMA0-ULTRA_DMA0 CPU_DMA1-ULTRA_DMA1
0001	CPU_DMA0-ULTRA_DMA0 CPU_DMA1-ULTRA_DMA2
0010	CPU_DMA0-ULTRA_DMA0 CPU_DMA1-ULTRA_DMA3
0011	CPU_DMA0-ULTRA_DMA0 CPU_DMA1-IDE_DMA
0100	CPU_DMA0-ULTRA_DMA1 CPU_DMA1-ULTRA_DMA2
0101	CPU_DMA0-ULTRA_DMA1 CPU_DMA1-ULTRA_DMA3
0110	CPU_DMA0-ULTRA_DMA1 CPU_DMA1-IDE_DMA
0111	CPU_DMA0-ULTRA_DMA2 CPU_DMA1-ULTRA_DMA3
1000	CPU_DMA0-ULTRA_DMA2 CPU_DMA1-IDE_DMA
1001	CPU_DMA0-ULTRA_DMA3 CPU_DMA1-IDE_DMA
OTHER	-

3. Remote Control Data Acknowledge Register (h'b2300000,h'12300000)

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	RMINT	RMACK
W	W	W	W	W	W	R	W

-Initial value: h'00

-D15-D9: The write value should always be 0.

-D9: Monitor of interrupt signal from infrared remote control receive controller

-D8: Acknowledge signal to infrared remote control receive controller.

Positive logic. This bit always read 0.

6.5. Remote Control Receive Control Block

Remote control receive control block receive an infrared remote control signal for home use and send 8-bit data to SH microcomputer and generate a receive interrupt request on receiving. Generated interrupt request is retained until 1 is written to bit 8 in a remote control data acknowledge register. When not using an interrupt, interrupt request can be confirmed by bit9 of remote control acknowledge register.

Receivable remote control format is as follows.

Format: NEC format

(custom code 8bit + custom reverse code 8bit+data code 8bit

+ data reverse code 8bit)

Custom code: h'FF

6.6. Interrupt

Table6.5 lists interrupt signals of the SolutionEngine used on the MSSIODB01. As listed in table6.5, interrupt from super I/O, IDE and remote control receive can be accepted. To use interrupt listed in table6.5, make interrupt connection jumper (JP3) closed. And set configuration to use the super I/O interruption.

Table6.5 MSSIODB01 usage interruption

Slot request interrupt	Connected device
Expansion Slot /IRQ1	Keyboard
Expansion Slot /IRQ2	-
Expansion Slot /IRQ3	Serial port
Expansion Slot /IRQ4	Mouse
Expansion Slot /IRQ5	IDE
Expansion Slot /IRQ6	Infrared Remote Control
Expansion Slot /IRQ7	-
Expansion Slot /IRQ8	-

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