REG[000h] Revision Code Register [2] (For S1D13506: Product Code=000100b, Revision Code=01b) RO

Product Code						Revision Code	
Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 1	Bit 0

REG[001h] Miscellaneous Register 1/0 RW

Register/ Memory Select	n/a	n/a	n/a	n/a	Reserved	Reserved	Reserved

REG[004h] General I/O Pins Configuration Register [3] 1/0 RW

Reserved	Reserved	Reserved	Reserved	GPIO3 Pin I/O Config	GPIO2 Pin I/O Config	GPIO1 Pin I/O Config	Reserved

REG[008h] General I/O Pins Control Register RW

Reserved	Reserved	Reserved	Reserved	GPIO3 Pin I/O Status	GPIO2 Pin I/O Status	GPIO1 Pin I/O Status	Reserved

REG[00Ch] MD Configuration Readback Register 0 RW

MD[7] Status	MD[6] Status	MD[5] Status	MD[4] Status	MD[3] Status	MD[2] Status	MD[1] Status	MD[0] Status

REG[00Dh] MD Configuration Readback Register 1 RW

MD[15] Status	MD[14] Status	MD[13] Status	MD[12] Status	MD[11] Status	MD[10] Status	MD[9] Status	MD[8] Status

REG[010h] Memory Clock Configuration Register [4] RW

n/a	n/a	n/a	MCLK Divide Slct	n/a	n/a	n/a	MCLK Source Slct

REG[014h] LCD Pixel Clock Configuration Register [5,6] RW

n/a	n/a	LCD PCLK Divide Select		n/a	n/a	LCD PCLK Source Select	
		Bit 1	Bit 0			Bit 1	Bit 0

REG[018h] CRT/TV Pixel Clock Configuration Register [7,8] RW

CRT/TV PCLK 2X Enable	n/a	CRT/TV PCLK Divide Slct		n/a	n/a	CRT/TV PCLK Source Slct	
		Bit 1	Bit 0			Bit 1	Bit 0

REG[01Ch] MediaPlug Clock Configuration Register [9,10] RW

n/a	n/a	MediaPlug Clock Divide Select		n/a	n/a	MediaPlug Clock Source Select	
		Bit 1	Bit 0			Bit 1	Bit 0

REG[01Eh] CPU To Memory Wait State Select Register [11] RW

n/a	n/a	n/a	n/a	n/a	n/a	CPU to Memory Wait State Select	
						Bit 1	Bit 0

REG[020h] Memory Configuration Register [12] RW

n/a	n/a	n/a	n/a	n/a	n/a	Memory Type	
						Bit 1	Bit 0

REG[021h] DRAM Refresh Rate Register [13,14] RW

Refresh Select		n/a	n/a	n/a	DRAM Refresh Rate		
Bit 1	Bit 0				Bit 2	Bit 1	Bit 0

REG[02Ah] DRAM Timing Control Register 0 [15] RW

DRAM Timing Control							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[02Bh] DRAM Timing Control Register 1 [15] RW

n/a	n/a	n/a	n/a	n/a	n/a	DRAM Timing Control	
						Bit 9	Bit 8

REG[030h] Panel Type Register [16] RW

EL Panel Mode Enable	n/a	Panel Data Width		Panel Data Format Select	Color/Mono Panel Select	Dual/Single Panel Select	TFT/Passive Panel Select
		Bit 1	Bit 0				

REG[031h] MOD Rate Register RW

n/a	n/a	MOD Rate					
		Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[032h] LCD Horizontal Display Width Register RW

n/a	LCD Horizontal Display Width						
	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[034h] LCD Horizontal Non-Display Period Register RW

n/a	n/a	n/a	LCD Horizontal Non-Display Period				
			Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[035h] TFT FPLINE Start Position Register RW

n/a	n/a	n/a	TFT FPLINE Start Position				
			Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[036h] TFT FPLINE Pulse Width Register [17] RW

LCD FPLINE Polarity Slct	n/a	n/a	n/a	TFT FPLINE Pulse Width			
				Bit 3	Bit 2	Bit 1	Bit 0

REG[038h] LCD Vertical Display Height Register 0 RW

LCD Vertical Display Height							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[039h] LCD Vertical Display Height Register 1 RW

n/a	n/a	n/a	n/a	n/a	n/a	LCD Vertical Display Height	
						Bit 9	Bit 8

REG[03Ah] LCD Vertical Non-Display Period Register RW

LCD VNDP Status(RO)	n/a	LCD Vertical Non-Display Period					
		Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[03Bh] TFT FPFRAME Start Position Register RW

n/a	n/a	TFT FPFRAME Start Position					
		Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[03Ch] TFT FPFRAME Pulse Width Register [18] RW

LCD FPFRAME Polarity Slct	n/a	n/a	n/a	n/a	TFT FPFRAME Pulse Width		
					Bit 2	Bit 1	Bit 0

REG[040h] LCD Display Mode Register [19] RW

LCD Display Blank	n/a	n/a	SwivelView Enable Bit 1	n/a	LCD Bit-per-pixel Select		
					Bit 2	Bit 1	Bit 0

REG[041h] LCD Miscellaneous Register RW

n/a	n/a	n/a	n/a	n/a	n/a	Dithering Disable	Dual Panel Buffer Disable

REG[042h] LCD Display Start Address Register 0 RW

LCD Display Start Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[043h] LCD Display Start Address Register 1 RW

LCD Display Start Address							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

REG[044h] LCD Display Start Address Register 2 RW

n/a	n/a	n/a	n/a	LCD Display Start Address			
				Bit 19	Bit 18	Bit 17	Bit 16

REG[046h] LCD Memory Address Offset Register 0 RW

LCD Memory Address Offset							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[047h] LCD Memory Address Offset Register 1 RW

n/a	n/a	n/a	n/a	n/a	LCD Memory Address Offset		
					Bit 10	Bit 9	Bit 8

REG[048h] LCD Pixel Panning Register [20] RW

n/a	n/a	n/a	n/a	Reserved	Reserved	LCD Pixel Panning	
						Bit 1	Bit 0

REG[04Ah] LCD Display FIFO High Threshold Control Register RW

n/a	n/a	LCD Display FIFO High Threshold					
		Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[04Bh] LCD Display FIFO Low Threshold Control Register RW

n/a	n/a	LCD Display FIFO Low Threshold					
		Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[050h] CRT/TV Horizontal Display Width Register RW

n/a	CRT/TV Horizontal Display Width						
	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[052h] CRT/TV Horizontal Non-Display Period Register RW

n/a	n/a	CRT/TV Horizontal Non-Display Period					
		Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[053h] CRT/TV HRTC Start Position Register RW

n/a	n/a	CRT/TV HRTC Start Position					
		Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[054h] CRT HRTC Pulse Width Register RW

CRT HRTC Polarity Slct	n/a	n/a	n/a	CRT HRTC Pulse Width			
				Bit 3	Bit 2	Bit 1	Bit 0

REG[056h] CRT/TV Vertical Display Height Register 0 RW

CRT/TV Vertical Display Height							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[057h] CRT/TV Vertical Display Height Register 1 RW

n/a	n/a	n/a	n/a	n/a	n/a	CRT/TV Vertical Display Height	
						Bit 9	Bit 8

REG[058h] CRT/TV Vertical Non-Display Period Register RW

CRT/TV VNDP Status (RO)	CRT/TV Vertical Non-Display Period						
	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[059h] CRT/TV VRTC Start Position Register RW

n/a	CRT/TV VRTC Start Position						
	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[05Ah] CRT/TV VRTC Pulse Width Register RW

CRT VRTC Polarity Slct	n/a	n/a	n/a	n/a	CRT VRTC Pulse Width		
					Bit 2	Bit 1	Bit 0

REG[05Bh] CRT/TV Output Control Register RW

n/a	n/a	TV Chrominance Filter Enable	TV Luminance Filter Enable	DAC Output Level Select	n/a	TV S-Video/ Composite Output Slct	TV PAL/ NTSC Output Slct

REG[060h] CRT/TV Display Mode Register [21] RW

CRT/TV Display Blank	n/a	n/a	n/a	n/a	CRT/TV Bit-per-pixel Select		
					Bit 2	Bit 1	Bit 0

REG[062h] CRT/TV Display Start Address Register 0 RW

CRT/TV Display Start Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[063h] CRT/TV Display Start Address Register 1 RW

CRT/TV Display Start Address							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

REG[064h] CRT/TV Display Start Address Register 2 RW

n/a	n/a	n/a	n/a	CRT/TV Display Start Address			
				Bit 19	Bit 18	Bit 17	Bit 16

REG[066h] CRT/TV Memory Address Offset Register 0 RW

CRT/TV Memory Address Offset							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[067h] CRT/TV Memory Address Offset Register 1 RW

n/a	n/a	n/a	n/a	n/a	CRT/TV Memory Address Offset		
					Bit 10	Bit 9	Bit 8

REG[068h] CRT/TV Pixel Panning Register [22] RW

n/a	n/a	n/a	n/a	Reserved	Reserved	CRT/TV Pixel Panning	
						Bit 1	Bit 1

REG[06Ah] CRT/TV Display FIFO High Threshold Control Register RW

n/a	n/a	CRT/TV Display FIFO High Threshold					
		Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[06Bh] CRT/TV Display FIFO Low Threshold Control Register RW

n/a	n/a	CRT/TV Display FIFO Low Threshold					
		Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[070h] LCD Ink/Cursor Control Register [23] RW

n/a	n/a	n/a	n/a	n/a	n/a	LCD Ink/Cursor Mode	
						Bit 1	Bit 0

REG[071h] LCD Ink/Cursor Start Address Register [24] RW

LCD Ink/Cursor Start Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[072h] LCD Cursor X Position Register 0 RW

LCD Cursor X Position							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[073h] LCD Curxor X Position Register 1 RW

LCD Cursor X Sign	n/a	n/a	n/a	n/a	n/a	LCD Cursor X Position	
						Bit 9	Bit 8

REG[074h] LCD Cursor Y Position Register 0 RW

LCD Cursor Y Position							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[075h] LCD Cursor Y Position Register 1 RW

LCD Cursor Y Sign	n/a	n/a	n/a	n/a	n/a	LCD Cursor Y Position	
						Bit 9	Bit 8

REG[076h] LCD Ink/Cursor Blue Color 0 Register RW

n/a	n/a	n/a	LCD Ink/Cursor Blue Color 0				
			Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[077h] LCD Ink/Cursor Green Color 0 Register RW

n/a	n/a	LCD Ink/Cursor Green Color 0					
		Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[078h] LCD Ink/Cursor Red Color 0 Register RW

n/a	n/a	n/a	LCD Ink/Cursor Red Color 0				
			Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[07Ah] LCD Ink/Cursor Blue Color 1 Register RW

n/a	n/a	n/a	LCD Ink/Cursor Blue Color 1				
			Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[07Bh] LCD Ink/Cursor Green Color 1 Register RW

n/.a	n/a	LCD Ink/Cursor Green Color 1					
		Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[07Ch] LCD Ink/Cursor Red Color 1 Register RW

n/a	n/a	n/a	LCD Ink/Cursor Red Color 1				
			Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[07Eh] LCD Ink/Cursor FIFO Thrshold Register RW

n/a	n/a	n/a	n/a	LCD Ink/Cursor FIFO Threshold			
				Bit 3	Bit 2	Bit 1	Bit 0

REG[080h] CRT/TV Ink/Cursor Control Register [25] RW

n/a	n/a	n/a	n/a	n/a	n/a	CRT/TV Ink/Cursor Mode	
						Bit 1	Bit 0

REG[081h] CRT/TV Ink/Cursor Start Address Register [26] RW

CRT/TV Ink/Cursor Start Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[082h] CRT/TV Cursor X Position Register 0 RW

CRT/TV Cursor X Position							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[083h] CRT/TV Cursor X Position Register 1 RW

CRT/TV Cursor X Sign	n/a	n/a	n/a	n/a	n/a	CRT/TV Cursor X Position	
						Bit 9	Bit 8

REG[084h] CRT/TV Cursor Y Position Register 0 RW

CRT/TV Cursor Y Position							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[085h] CRT/TV Cursor Y Position Register 1 RW

CRT/TV Cursor Y Sign	n/a	n/a	n/a	n/a	n/a	CRT/TV Cursor Y Position	
						Bit 9	Bit 8

REG[086h] CRT/TV Ink/Cursor Blue Color 0 Register RW

n/a	n/a	n/a	CRT/TV Ink/Cursor Blue Color 0				
			Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[087h] CRT/TV Ink/Cursor Green Color 0 Register RW

n/a	n/a	CRT/TV Ink/Cursor Green Color 0					
		Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[088h] CRT/TV Ink/Cursor Red Color 0 Register RW

n/a	n/a	n/a	CRT/TV Ink/Cursor Red Color 0				
			Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[08Ah] CRT/TV Ink/Cursor Blue Color 1 Register RW

n/a	n/a	n/a	CRT/TV Ink/Cursor Blue Color 1				
			Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[08Bh] CRT/TV Ink/Cursor Green Color 1 Register RW

n/a	n/a	CRT/TV Ink/Cursor Green Color 1					
		Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[08Ch] CRT/TV Ink/Cursor Red Color 1 Register RW

n/a	n/a	n/a	CRT/TV Ink/Cursor Red Color 1				
			Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[08Eh] CRT/TV Ink/Cursor FIFO Threshold Register RW

n/a	n/a	n/a	n/a	CRT/TV Ink/Cursor FIFO Threshold			
				Bit 3	Bit 2	Bit 1	Bit 0

REG[100h] BitBlt Control Register 0 [27] RW

BitBlt Active Status	BitBlt FIFO Not Empty Status (RO)	BitBlt FIFO Half Full Status (RO)	BitBlt FIFO Full Status (RO)	n/a	n/a	BitBlt Destination Linear Slct	BitBlt Source Linear Slct

REG[101h] BitBlt Control Register 1 RW

n/a	n/a	n/a	BitBlt FIFO Depth	n/a	n/a	n/a	BitBlt Color Format Slct

REG[102h] BitBlt ROP Code/Color Expansion Register [28] RW

n/a	n/a	n/a	n/a	BitBlt ROP Code			
				Bit 3	Bit 2	Bit 1	Bit 0

REG[103h] BitBlt Operation Register [29] RW

n/a	n/a	n/a	n/a	BitBlt Operation			
				Bit 3	Bit 2	Bit 1	Bit 0

REG[104h] BitBlt Source Start Address Register 0 [30] RW

BitBlt Source Start Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[105h] BitBlt Source Start Address Register 1 [30] RW

BitBlt Source Start Address							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

REG[106h] BitBlt Source Start Address Register 2 [30] RW

n/a	n/a	n/a	BitBlt Source Start Address				
			Bit 20	Bit 19	Bit 18	Bit 17	Bit 16

REG[108h] BitBlt Destination Start Address Register 0 RW

BitBlt Destination Start Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[109h] BitBlt Destination Start Address Register 1 RW

BitBlt Destination Start Address							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

REG[10Ah] BitBlt Destination Start Address Register 2 RW

n/a	n/a	n/a	BitBlt Destination Start Address				
			Bit 20	Bit 19	Bit 18	Bit 17	Bit 16

REG[10Ch] BitBlt Memory Address Offset Register 0 RW

BitBlt Memory Address Offset							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[10Dh] BitBlt Memory Address Offset Register 1 RW

n/a	n/a	n/a	n/a	n/a	BitBlt Memory Address Offset		
					Bit 10	Bit 9	Bit 8

REG[110h] BitBlt Width Register 0 RW

BitBlt Width							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[111h] BitBlt Width Register 1 RW

n/a	n/a	n/a	n/a	n/a	n/a	BitBlt Width	
						Bit 9	Bit 8

REG[112h] BitBlt Height Register 0 RW

BitBlt Height							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[113h] BitBlt Height Register 1 RW

n/a	n/a	n/a	n/a	n/a	n/a	BitBlt Height	
						Bit 9	Bit 8

REG[114h] BitBlt Backgroud Color Register 0 RW

BitBlt Background Color							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[115h] BitBlt Background Color Register 1 RW

BitBlt Background Color							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

REG[118h] BitBlt Foreground Color Register 0 RW

BitBlt Foreground Color							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[119h] BitBlt Foreground Color Register 1 RW

BitBlt Foreground Color							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

REG[1E0h] Look-Up Table Mode Register [31] RW

n/a	n/a	n/a	n/a	n/a	n/a	LUT Mode	
						Bit 1	Bit 0

REG[1E2h] Look-Up Table Address Register							RW
LUT Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[1E4h] Look-Up Table Data Register							RW
LUT Data				n/a	n/a	n/a	n/a
Bit 3	Bit 2	Bit 1	Bit 0				

REG[1F0h] Power Save Configuration Register							RW
n/a	n/a	n/a	Reserved	n/a	n/a	n/a	Power Save Mode Enbl

REG[1F1h] Power Save Status Register							RO
n/a	n/a	n/a	n/a	n/a	n/a	LCD Power Save Status	Memory Controller Power Save Status

REG[1F4h] CPU-to-Memory Access Watchdog Timer Register							RW
n/a	n/a	CPU-to-Memory Access Watchdog Timer					
		Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

REG[1FCh] Display Mode Register [32]							RW
n/a	SwivelView Enable Bit 0	n/a	n/a	n/a	Display Mode Select		
					Bit 2	Bit 1	Bit 0

REG[1000h] MediaPlug LCMD Register							RW
MediaPlug LCMD							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

REG[1002h] MediaPlug Reserved LCMD Register							RW
MediaPlug Reserved LCMD							
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24

REG[1004h] MediaPlug CMD Register							RW
MediaPlug CMD							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

REG[1006h] MediaPlug Reserved CMD Register							RW
MediaPlug Reserved CMD							
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24

REG[1008h] to REG[1FFEh], even address MediaPlug Data Registers							RW
MediaPlug Data							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

A20-A0 = 100000h-1FFFFEh, even address BitBlt Data Register 0							RW
BitBlt Data							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

1 N/A bits should be written 0.
Reserved bits must be written 0.

2 REG[000h] These bits are used to identify the S1D13506. For the S1D13506 the product code should be 4; the revision code should be 1. The host interface must be enabled before reading this register (set REG[001] b7=0).

3 REG[004h] MA[11:9]/GPIO[1:3] Pin Functionality

MD14 on Reset	MD[7:6] on Reset	Pin		
		MA9/GPIO3	MA10/GPIO1	MA11/GPIO2
0	00	GPIO3	GPIO1	GPIO2
0	01	MA9	GPIO1	GPIO2
0	10	MA9	GPIO1	GPIO2
0	11	MA9	MA10	MA11

MD14 on Reset	MD[7:6] on Reset	Pin		
		MA9/GPIO3	MA10/GPIO1	MA11/GPIO2
1	00	GPIO3	GPIO1	VMPEPWR
1	01	MA9	GPIO1	VMPEPWR
1	10	MA9	GPIO1	VMPEPWR
1	11	MA9	MA10	MA11

4 REG[010h] MCLK Source Select

MCLK Source Select	MCLK Source
0	CLKI
1	BUSCLK

5 REG[014h] LCD PCLK Divide Select

LCD PCLK Divide Select Bits [1:0]	LCD PCLK Source to LPCLK Frequency Ratio
00	1:1
01	2:1
10	3:1
11	4:1

6 REG[014h] LCD PCLK Source Select

LCD PCLK Source Select Bits [1:0]	LCD PCLK Source
00	CLKI
01	BUSCLK
10	CLKI2
11	MCLK

7 REG[018h] CRT/TV PCLK Divide Select

CRT/TV PCLK Divide Select Bits [1:0]	CRT/TV PCLK Source to DPCLK Frequency Ratio
00	1:1
01	2:1
10	3:1
11	4:1

8 REG[018h] CRT/TV PCLK Source Select

CRT/TV PCLK Source Select Bits [1:0]	CRT/TV PCLK Source
00	CLKI
01	BUSCLK
10	CLKI2
11	MCLK

9 REG[01Ch] MediaPlug Clock Divide Select

MediaPlug Clock Divide Select Bits [1:0]	MediaPlug Clock Source to CRT/TV Pixel Clock Frequency Ratio
00	1:1
01	2:1
10	3:1
11	4:1

10 REG[01Ch] MediaPlug Clock Source Select

MediaPlug Clock Source Select Bits [1:0]	MediaPlug Clock Source
00	CLKI
01	BUSCLK
10	CLKI2
11	MCLK

11 REG[01Eh] Minimum Memory Timing Selection

Wait State Bits [1:0]	Condition
00	no restrictions
01	2 * period (MCLK) - 4ns > period(BCLK)
10	period(MCLK) - 4ns > period(BCLK)
11	Reserved

12 REG[020h] Memory Type Select

Memory Type Bits [1:0]	Memory Type
00	EDO-DRAM with 2-CAS#
01	FPM-DRAM with 2-CAS#
10	EDO-DRAM with 2-WE#
11	FPM-DRAM with 2-WE#

13 REG[021h] DRAM Refresh Select

DRAM Refresh Select Bits [1:0]	DRAM Refresh Type
00	CBR Refresh
01	Self-Refresh
1X	No Refresh

14 REG[021h] DRAM Refresh Rate

DRAM Refresh Rate Bits [2:0]	MCLK Source Divide Amount	Refresh Rate for 40MHz MCLK Source	DRAM Refresh Time/256 cycles
000	64	625 kHz	0.4 ms
001	128	312 kHz	0.8 ms
010	256	156 kHz	1.6 ms
011	512	78 kHz	3.3 ms
100	1024	39 kHz	6.6 ms
101	2048	20 kHz	13.1 ms
110	4096	10 kHz	26.2 ms
111	8192	5 kHz	52.4 ms

15 REG[02Ah], REG[02Bh] DRAM Timing Control Registers

DRAM Type	DRAM Speed (ns)	MCLK Frequency (MHz)	DRAM Timing Control Reg 0	DRAM Timing Control Reg 1
EDO	50	40	01h	01h
	50	33	01h	01h
	60		01h	01h
	50	30	12h	02h
	60		01h	01h
	70		00h	00h
	50	25	12h	02h
	60		12h	02h
	70		01h	01h
	80		00h	01h
	50	20	12h	02h
	60		12h	02h
	70		12h	02h
	80		01h	01h
FPM	50	25	12h	02h
	60		01h	01h
	50	20	12h	02h
	60		12h	02h
	70		11h	02h
	80		01h	01h

16 REG[030h] Panel Data Width

Panel Data Width Bits [1:0]	Passive LCD Panel Data Width	TFT/D-TFD Panel Data Width
00	4-bit	9-bit
01	8-bit	12-bit
10	16-bit	18-bit (64K color)
11	Reserved	Reserved

17 REG[036h] LCD FPLINE Polarity Select

LCD FPLINE Polarity Select	Passive LCD FPLINE Polarity	TFT FPLINE Polarity
0	active high	active low
1	active low	active high

18 REG[03Ch] LCD FPFRAME Polarity Select

LCD FPFRAME Polarity Select	Passive LCD FPFRAME Polarity	TFT FPFRAME Polarity
0	active high	active low
1	active low	active high

19 REG[040h] LCD Bit-per-pixel Select

Bit-per-pixel Select Bits [1:0]	Color Depth (bpp)
000-001	Reserved
010	4 bpp
011	8 bpp
100	15 bpp
101	16 bpp
110-111	Reserved

20 REG[048h] LCD Pixel Planning

Color Depth	Screen 2 Pixel Panning Bits Used
4 bpp	Bits [1:0]
8 bpp	Bit 0
15/16 bpp	---

21 REG[060h] CRT/TV Bit-per-pixel Select

Bit-per-pixel Select Bits 1:0	Bit-per-pixel (bpp)
000-001	Reserved
010	4 bpp
011	8 bpp
100	15 bpp
101	16 bpp
110-111	Reserved

22 REG[068h] CRT/TV Pixel Planning

Color Depth	Screen 2 Pixel Panning Bits Used
4 bpp	Bits [1:0]
8 bpp	Bit 0
15/16 bpp	---

23 REG[070h] LCD Ink/Cursor Selection

LCD Ink/Cursor Bits [1:0]	Mode
00	Inactive
01	Cursor
10	Ink
11	Reserved

24 REG[071h] LCD Ink/Cursor Start Address Encoding

LCD Ink/Cursor Start Address Bits [7:0]	Start Address
0	Memory Size - 1024
n = 255...1	Memory Size - n * 8192

25 REG[080h] CRT/TV Ink/Cursor Selection

CRT/TV Ink/Cursor Bits [1:0]	Mode
00	Inactive
01	Cursor
10	Ink
11	Reserved

26 REG[081h] CRT/TV Ink/Cursor Start Address Encoding

CRT/TV Ink/Cursor Start Address Bits [7:0]	Start Address
0	Memory Size - 1024
n = 255...1	Memory Size - n * 8192

27 REG[100h] BitBlt Active Status

BitBlt Active Status		State
Write	Read	
0	0	Idle
0	1	Reserved
1	0	Initiatiating operation
1	1	Operation in progress

28 REG[102h] BitBlt ROP Code/Color Expansion Function Selection

BitBlt ROP Code Bits [3:0]	Boolean Function for Write Blit and Move Blit	Boolean Function for Pattern Fill	Start Bit Positon for Color Expansion
0000	0 (Blackness)	0 (Blackness)	bit 0
0001	~S . ~D or ~(S + D)	~P . ~D or ~(P + D)	bit 1
0010	~S . D	~P . D	bit 2
0011	~S	~P	bit 3
0100	S . ~D	P . ~D	bit 4
0101	~D	~D	bit 5
0110	S ^ D	P ^ D	bit 6
0111	~S + ~D or ~(S . D)	~P + ~D or ~(P . D)	bit 7
1000	S . D	P . D	bit 0
1001	~(S ^ D)	~(P ^ D)	bit 1
1010	D	D	bit 2
1011	~S + D	~P + D	bit 3
1100	S	P	bit 4
1101	S + ~D	P + ~D	bit 5
1110	S + D	P + D	bit 6
1111	1 (Whiteness)	1 (Whiteness)	bit 7

29 REG[103h] BitBlt Operation Selection

BitBlt Operation Bits [3:0]	Blit Operation
0000	Write Blit with ROP.
0001	Read Blit.
0010	Move Blit in positive direction with ROP.
0011	Move Blit in negative direction with ROP.
0100	Transparent Write Blit.
0101	Transparent Move Blit in positive direction.
0110	Pattern Fill with ROP.
0111	Pattern Fill with transparency.
1000	Color Expansion.
1001	Color Expansion with transparency.
1010	Move Blit with Color Expansion.
1011	Move Blit with Color Expansion and transparency.
1100	Solid Fill.
Other combinations	Reserved

30 REG[104h],[105h],[106h] BitBlt Source Start Address Selection

Color Format	Pattern Base Address[20:0]	Pattern Line Offset[2:0]	Pixel Offset[3:0]
8 bpp	BitBlt Source Start Address[20:6], 6'b0	BitBlt Source Start Address[5:3]	1'b0, BitBlt Source Start Address[2:0]
16 bpp	BitBlt Source Start Address[20:7], 7'b0	BitBlt Source Start Address[6:4]	BitBlt Source Start Address[3:0]

31 REG[1E0h] LUT Mode Selection

LUT Mode Bits [1:0]	Read	Write
00	LCD LUT	LCD and CRT/TV LUT's
01	LCD LUT	LCD LUT
10	CRT/TV LUT	CRT/TV LUT
11	Reserved	Reserved

32 REG[1FCh] Display Mode Select

Display Mode Select Bits [2:0]	Display Mode Enabled
000	no display
001	LCD only
010	CRT only
011	Double CRT and LCD
100	TV with flicker filter off
101	Double Display TV with flicker filter off and LCD
110	TV with flicker filter on
111	Double Display TV with flicker filter on and LCD