MQ322-05

EPSON

# *Application Manual*

## Real Time Clock Module

# RTC-8564JE/NB

| Model | Product Number |
|---|---|
| RTC-8564JE | Q4185647x000100 |
| RTC-8564NB | Q4185649x000200 |


SEIKO EPSON CORPORATION


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# CONTENTS

I²C-Bus Interface Real Time Clock Module

# RTC - 8564 JE/NB

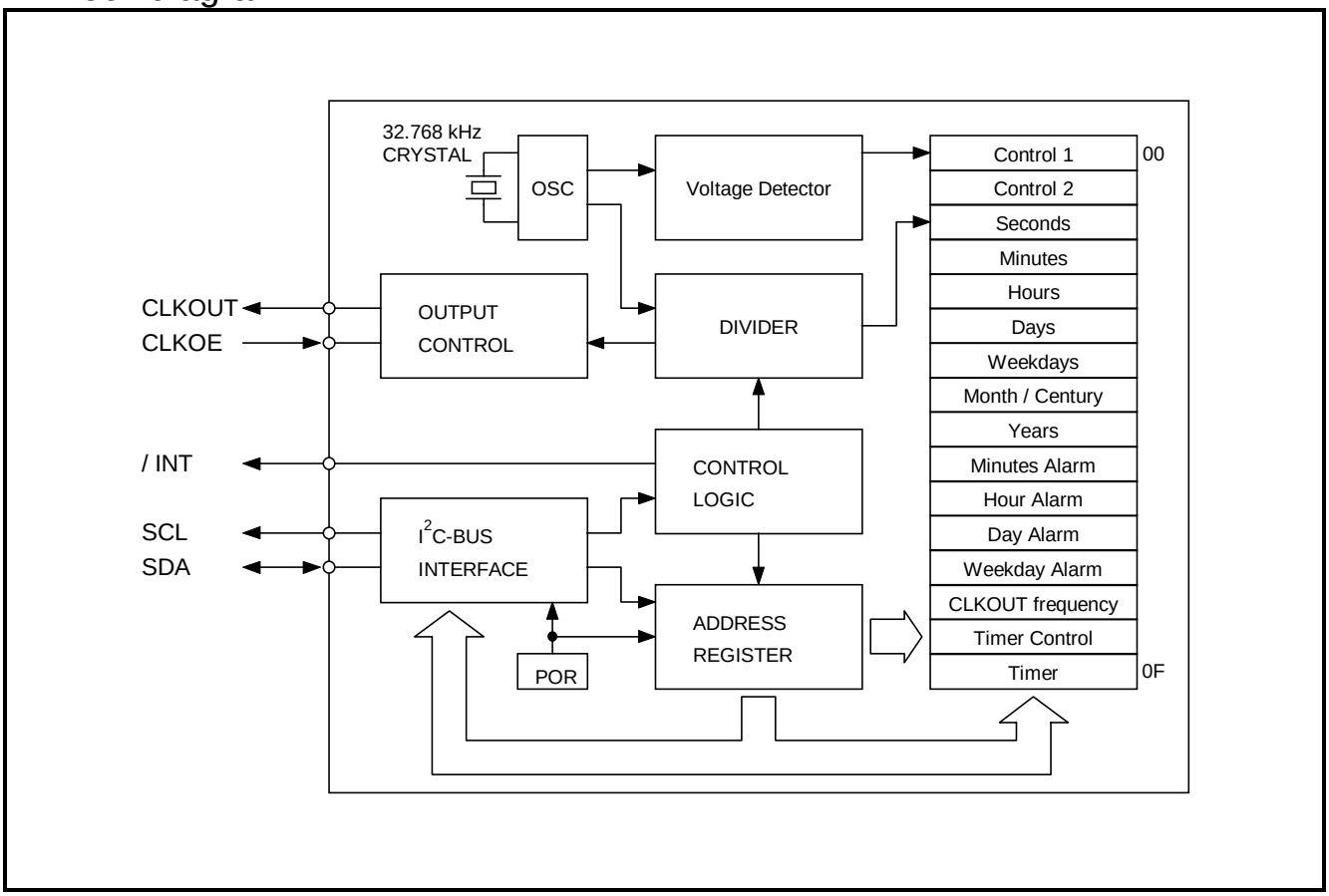
- Built-in crystal oscillator running at 32.768 kHz
- Compliant with I²C high-speed bus specifications ( 400 kHz )
- Equipped with alarm, timer, and frequency output ( 32.768 kHz, 1024 Hz, 32 Hz, 1 Hz ) features
- Inclusion of century bit to enable correct date even after year 2000
- Wide range of interface voltage between 1.8 V and 5.5 V
- Wide range of clock voltage between 1.0 V and 5.5 V ( Ta= –20 °C to +70 °C )
- Low power consumption at 275 nA / 3.0 V (Typ.)



## 1. Overview

This module is a serial interface real time clock that has a built-in crystal oscillator.
The module offers many functions such as calendar clock, alarm, and timer. All of them can be controlled with a two (2) lines interface. Also, the regular frequency output can be selected from programs.
Because this module has multiple features packaged in the same surface, it is ideally suited for applications such as mobile phones, handy terminals or other small electronic systems.

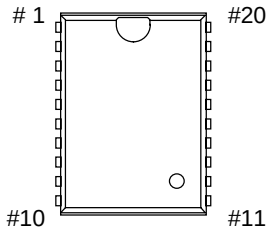
## 2. Block diagram



# 3. Terminal description

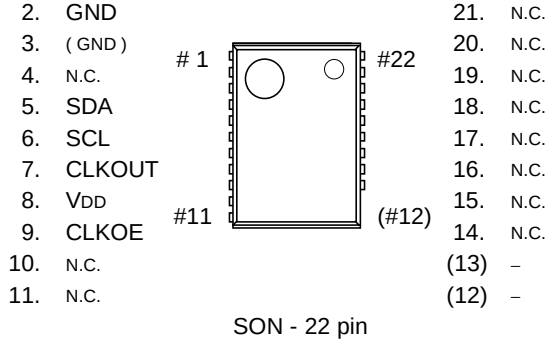
## 3.1. Terminal connections

RTC - 8564 JE




VSOJ - 20 pin

RTC - 8564 NB




SON - 22 pin

## 3.2. Terminal functions

| Signal name | Pin No. | | I/O | Signal description |
|---|---|---|---|---|
| | 8564JE VSOJ-20pin | 8564NB SON-22pin | | |
| CLKOE | 3 | 9 | Input | This pin control the frequency output from CLKOUT pin. When this pin is LOW ,frequency output is inhibited by all means. When this pin is HIGH and FE-Bit is "1", frequency output is available. |
| VDD | 4 | 8 | – | This pin connects to the + power source. |
| CLKOUT | 5 | 7 | Output | This pin outputs frequency ( 32.768 kHz, 1024 Hz, 32 Hz, 1 Hz ) selected by the program. The pin is an C-MOS terminal. When initial power is supplied (power supply starting from 0 V ), the power-on reset function causes 32.768 kHz to be output. When output stops, the CLKOUT pin goes to LOW. Control of CLKOE pin is necessaryto control this function justly. |
| SCL | 6 | 6 | Input | For input of the serial clock. |
| SDA | 7 | 5 | Bi-Directional | This pin synchronizes with a serial clock and input/output address, data, acknowledge bit, etc. The pin is an open-drain in output mode. Be sure to use the appropriate pull-up resistors according to the capacitance of the signal lines. |
| (GND) | 8 | 3 | – | This pin has the same voltage level as GND. Do not connect externally. |
| GND | 9 | 2 | – | This pin connects to the ground. |
| / INT | 10 | 1 | Output | This pin outputs an interrupt signal such as alarm and timer. The pin is an open-drain terminal. |
| N.C. | 1, 2, 11 – 20 | 4, 10, 11 14 – 22 | – | This pin is not connected internally. But , In RTC-8564NB( SON-22pin ), all pins from 14 pin to 22 pin are connected with inside frame mutually. Use OPEN, or GND or VDD to connect. |

∗ Be sure to connect a filter capacity of at least 0.1 μF closely between VDD and GND.

## 4. Absolute maximum ratings

GND=0 V

| Parameter | Symbol | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | Between $V_{DD}$ and GND | –0.5 | +6.5 | V |
| Supply Voltage | $I_{DD}$ | $V_{DD}$ pin | –50 | 50 | mA |
| Input Voltage | $V_I$ | Input pin | GND–0.5 | $V_{DD}$ +0.5 | V |
| Output Voltage | $V_O$ | / INT pin | GND–0.5 | $V_{DD}$ +0.5 | V |
| DC Input Current | $I_I$ | | –10 | 10 | mA |
| DC Output Current | $I_O$ | | –10 | 10 | mA |
| Storage Temperature Range | $T_{STG}$ | Stored bare product after unpacking | –55 | +125 | °C |

## 5. Recommended operating conditions

GND=0 V

| Parameter | Symbol | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Supply voltage range | $V_{DD}$ | $I^2C$-BUS access at 400 kHz | 1.8 | 5.5 | V |
| Clock voltage range | $V_{DD}$ | | $V_{LOW}$ | 5.5 | V |
| Operating temperature range | $T_{OPR}$ | No condensation | –40 | +85 | °C |

## 6. Frequency characteristics

GND=0 V

| Parameter | Symbol | Condition | Max. | Unit |
|---|---|---|---|---|
| Frequency precision | Δf / fo | Ta = +25 °C<br>$V_{DD}$ =3.0 V | 5 ± 23 (*1) | × $10^{-6}$ |
| Frequency voltage characteristics | f / V | Ta = +25 °C<br>$V_{DD}$ = 1.0 V to 5.5 V | ± 2 Max. | × $10^{-6}$ / V |
| Frequency temperature characteristics | Top | Ta = –10 to +70 °C<br>$V_{DD}$ = 3.0 V<br>Reference at +25 °C | +10 / –120 | × $10^{-6}$ |
| Oscillation startup-up time | tSTA | Ta = +25 °C<br>$V_{DD}$ = 1.8 V | 3 Max. | s |
| Aging | fa | Ta = +25 °C<br>$V_{DD}$ = 3.0 V ; first year | ± 5 Max. | × $10^{-6}$ / year |

*1) Equivalent to 1 minute of monthly deviation. ( excluding offset )

## 7. Electrical characteristics

### 7.1. DC electrical characteristics

∗ If not specifically indicated, GND=0 V, $V_{DD}$=1.8 V to 5.5 V , Ta= –40 °C to +85 °C

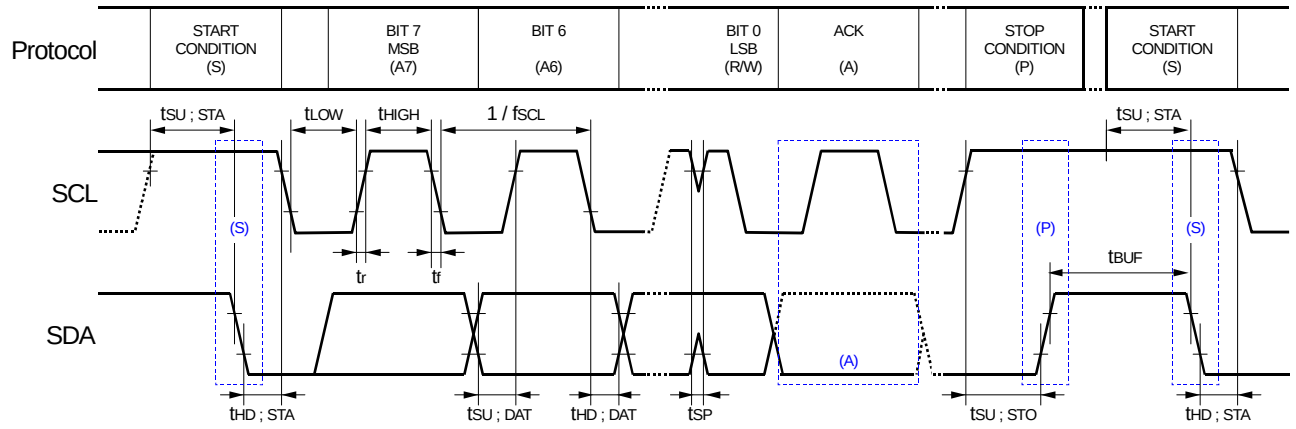
| Parameter | Symbol | Pin | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Power current (during access) | $I_{DDO}$ | | $f_{SCL}$=400 kHz<br>$f_{SCL}$=100 kHz | | | 800<br>200 | µA<br>µA |
| Power current (not during access) | $I_{DD}$ | | $f_{SCL}$=0 Hz, $V_{DD}$=5.0 V<br>$f_{SCL}$=0 Hz, $V_{DD}$=3.0 V<br>$f_{SCL}$=0 Hz, $V_{DD}$=2.0 V | | 330<br>275<br>250 | 800<br>700<br>650 | nA<br>nA<br>nA |
| Power current (not during access) (CLKOUT=32.768 kHz, LOAD is 0 pF) | $I_{DD32K}$ | | $f_{SCL}$=0 Hz, $V_{DD}$=5.0 V<br>$f_{SCL}$=0 Hz, $V_{DD}$=3.0 V<br>$f_{SCL}$=0 Hz, $V_{DD}$=2.0 V | | 2.5<br>1.5<br>1.1 | 3.4<br>2.2<br>1.6 | µA<br>µA<br>µA |
| "L" input voltage | $V_{IL}$ | | | GND – 0.5 | | 0.3 × $V_{DD}$ | V |
| "H" input voltage | $V_{IH}$ | | | 0.7 × $V_{DD}$ | | $V_{DD}$ + 0.5 | V |
| "L" output voltage | $I_{OL}$ (SDA) | SDA | $V_{OL}$=0.4 V, $V_{DD}$=5 V | –3 | | | mA |
| "L" output current | $I_{OL}$ (/INT) | / INT | $V_{OL}$=0.4 V, $V_{DD}$=5 V | –1 | | | mA |
| "L" output current | $I_{OL}$ (CLKOUT) | CLKOUT | $V_{OL}$=0.4 V, $V_{DD}$=5 V | –1 | | | mA |
| "H" output current | $I_{OH}$ (CLKOUT) | CLKOUT | $V_{OH}$=4.6 V, $V_{DD}$=5 V | | | 1 | mA |
| Leakage current | $I_{LO}$ | | $V_O$=$V_{DD}$ or GND | –1 | | 1 | µA |
| Low voltage detection | $V_{LOW}$ | | Ta= –40 °C to +85 °C<br>Ta= –20 °C to +70 °C | | 0.9<br>0.9 | 1.1<br>1.0 | V |

## 7.2. AC electrical characteristics

∗ If not specifically indicated, GND=0 V, $V_{DD}$=1.8 V to 5.5 V , Ta= –40 °C to +85 °C

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| SCL clock frequency | $f_{SCL}$ | | | | 400 | kHz |
| Start condition set-up time | $t_{SU;\ STA}$ | | 0.6 | | | µs |
| Start condition hold time | $t_{HD;\ STA}$ | | 0.6 | | | µs |
| Data set-up time | $t_{SU;\ DAT}$ | | 100 | | | ns |
| Data hold time | $t_{HD;\ DAT}$ | | 0 | | | ns |
| Stop condition set-up time | $t_{SU;\ STO}$ | | 0.6 | | | µs |
| Bus free time between a STOP and START condition | $t_{BUF}$ | | 1.3 | | | µs |
| SCL "L" time | $t_{LOW}$ | | 1.3 | | | µs |
| SCL "H" time | $t_{HIGH}$ | | 0.6 | | | µs |
| SCL and SDA rise time | tr | | | | 0.3 | µs |
| SCL and SDA fall time | tf | | | | 0.3 | µs |
| Tolerance spike time on bus | $t_{SP}$ | | | | 50 | ns |

Timing chart




Note : $I^2C$ access time between a START and a START condition or between a START and a STOP condition to this device must be less than one second.

# 8. How to use

## 8.1. Register table

| Address | Function | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 00 | Control 1 | TEST | 0 | STOP | 0 | TEST | 0 | 0 | 0 |
| 01 | Control 2 | 0 | × | 0 | TI / TP | AF | TF | AIE | TIE |
| 02 | Seconds | VL | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| 03 | Minutes | × | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| 04 | Hours | × | × | 20 | 10 | 8 | 4 | 2 | 1 |
| 05 | Days | × | × | 20 | 10 | 8 | 4 | 2 | 1 |
| 06 | Weekdays | × | × | × | × | × | 4 | 2 | 1 |
| 07 | Months / Century | C | × | × | 10 | 8 | 4 | 2 | 1 |
| 08 | Years | 80 | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| 09 | Minute Alarm | AE | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| 0A | Hour Alarm | AE | × | 20 | 10 | 8 | 4 | 2 | 1 |
| 0B | Day Alarm | AE | × | 20 | 10 | 8 | 4 | 2 | 1 |
| 0C | Weekday Alarm | AE | × | × | × | × | 4 | 2 | 1 |
| 0D | CLKOUT frequency | FE | × | × | × | × | × | FD1 | FD0 |
| 0E | Timer control | TE | × | × | × | × | × | TD1 | TD0 |
| 0F | Timer | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |

Notes ;

(1) When the power is turned on initially, the FD1 and FD0 bits are cleared to 0. Also, FE and VL bits are set to 1, but because other the register values of other bits are unknown, always make their initial settings. When doing so, do not make settings for date and time that are impossible. We do not guarantee proper operation of the clock for such settings.

(2) While there is a bit at address 00 for setting the test mode, the test mode is a special operation mode that is used by EPSON for testing devices. Be sure not to set it to 1. If it is set to the test mode, all operations of the device will not be guaranteed. Therefore, be careful when access to address 00.

(3) Be sure to set bit '0' of address 00,01 (Control1,2) to zero.

(4) All count data at address 02 through 05 and 08 through 0B is in the BCD format.

(5) Write to bit '×' is not possible, and its read-out value is not fixed. Be sure to mask it after bit '×' is read out.

## 8.2. Register description

### 8.2.1. Control register 1

| Address | Function | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 00 | Control 1 | TEST | 0 | STOP | 0 | TEST | 0 | 0 | 0 |

- TEST

  The two TEST bits are for testing devices. Therefore be sure to set them to zeros. If they are accidentally set to 1, they may immediately modify the clock data or result in abnormal time.

- STOP

  When this bit becomes zero, the device's time function operates. When it is set to 1, all internal count down chain are goes into the zero clear state. If it is cleared together with the time reporting, the time can be adjusted accurately up to one second. As for output of CLKOUT,
  STOP doesn't affect frequency output of 32768 Hz.But output stops at the time of frequency setting except 32768 Hz by STOP =1.

8.2.2. Control register 2

| Address | Function | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 01 | Control 2 | 0 | × | 0 | TI / TP | AF | TF | AIE | TIE |

- TI/TP ( Interrupt Signal Output Mode Select. Interrupt / Periodic )
  If this bit is set to 0, when the timer counts down in the single operation mode and becomes zero, it sets the TF flag and then stops. If this bit is set to 1, when the timer in the repeat mode becomes zero, it sets the TF flag, and it furthermore reload the initial value and repeat to count down. As long as the TF flag is not cleared, the set is maintained.

- AF ( Alarm Flag )
  This is a flag bit which goes into the set state when an alarm occurs.

- TF ( Timer Flag )
  This is a flag bit which goes into the set state when the timer counts down within the specified cycle and becomes zero.

- AIE ( Alarm Interrupt Enable )
  This bit determines whether to output the alarm flag state to the /INT pin. When it is set to 1, AF=1 then /INT becomes LOW. When it is set to 0, the information is not output to the /INT pin.

- TIE ( Timer Interrupt Enable )
  This bit determines whether to output the Timer flag state to the /INT pin. When it is set to 1, TF=1 then /INT becomes LOW. When it is set to 0, the information is not output to the /INT pin.

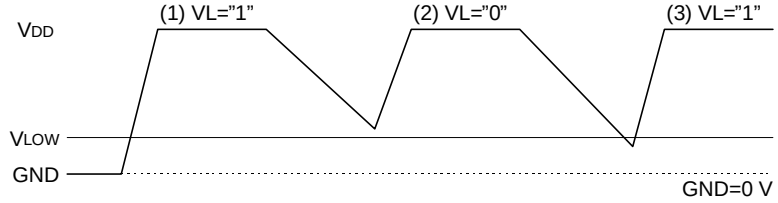
(Note)
The /INT pin outputs the logical sum of the respective signal of alarm interrupt and timer interrupt. When an interrupt occurs, the AF/TF flag is read out. Therefore, be sure to check to see which interrupt event has occurred.When alarm and timer are both prohibited . The /INT pin will not become LOW active. If all hardware interrupts cannot be used due to system constraints, after the above setup, be sure to use the software to monitor the interrupt flags for AF and TF.

8.2.3. Clock and calendar registers, and VL bit and century bit

| Address | Function | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 02 | Seconds | VL | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| 03 | Minutes | × | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| 04 | Hours | × | × | 20 | 10 | 8 | 4 | 2 | 1 |
| 05 | Days | × | × | 20 | 10 | 8 | 4 | 2 | 1 |
| 06 | Weekdays | × | × | × | × | × | 4 | 2 | 1 |
| 07 | Months / Century | C | × | × | 10 | 8 | 4 | 2 | 1 |
| 08 | Years | 80 | 40 | 20 | 10 | 8 | 4 | 2 | 1 |

If data and time are set to impossible values, the clock cannot operate correctly. Therefore pay attention when handling them.

- VL ( Voltage Low bit )
  This is the bit for detecting low voltage. When the power source's voltage drops below VLOW[V]*, this flag is set to 1.
  After the initial power-on, it is set to 1. If this flag is set to 1 after recovery from the backup state, this means during the backup the power was low, and all data need to be initialized.
  But this bit is intended to detect the situation when $V_{DD}$ is decreasing slowly for example under battery operation.
  In other words, chattering doesn't detect it.
  However, because this bit is write cleared regardless of the data, before performing a write to this register, be sure to read out its value.
  ∗See the description on DC electrical characteristics.




(1) VL="1" as result of initial supply of power
(2) When the power supply is low but voltage not dropping to $V_{LOW}$, VL remains at "0" with no change
(3) When the power supply is low and voltage dropping below $V_{LOW}$, VL becomes "1".

∗ The value of the VL bit in (2) and (3) need to be zero cleared in (1).

• C ( Century bit )

This bit indicates change of century. When the year digit data overflows from 99 to 00, this bit is set. By presetting it to 0 while still in the 20th century, it will be set in year 2000, but in fact the first year in the 21 century should be 2001.

• Weekdays registers ( Example for allotment of a day. )

| Address | Function | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Week |
|---|---|---|---|---|---|---|---|---|---|
| 06 | Weekdays | × | × | × | × | 0 | 0 | 0 | SUN |
| | | × | × | × | × | 0 | 0 | 1 | MON |
| | | × | × | × | × | 0 | 1 | 0 | TUE |
| | | × | × | × | × | 0 | 1 | 1 | WED |
| | | × | × | × | × | 1 | 0 | 0 | THU |
| | | × | × | × | × | 1 | 0 | 1 | FRI |
| | | × | × | × | × | 1 | 1 | 0 | SAT |

8.2.4. Alarm registers

| Address | Function | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 09 | Minute Alarm | AE | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| 0A | Hour Alarm | AE | × | 20 | 10 | 8 | 4 | 2 | 1 |
| 0B | Day Alarm | AE | × | 20 | 10 | 8 | 4 | 2 | 1 |
| 0C | Weekday Alarm | AE | × | × | × | × | 4 | 2 | 1 |

• AE

This is the alarm control bit. There is an MSB for each register of minute alarm, hour alarm, day alarm, and day of week alarm. When this bit is set to 1, the appropriate register will be set to have the alarm unconditionally and regardless of the data, and this device is regarded as to have the circuitry working.
When the hour digit and the AE of data are set, alarm will occur at the specified minute regardless of the date and time. In other words the alarm will occur at the specified minute of every hour. Similarly, when minute and hour are set to AE, alarm occurs at the specified date. Therefore, by combining them in this way a highly versatile alarm can be set. When all of the bits are set to AE, no alarm will occur.

Additional information on the alarm function:
Even when the alarm is turned on for a long time, this device clears the flag when the alarm occurs once, and so no more further alarm will occur under the same condition. This means in the same day when the alarm condition is met, once the alarm flag is cleared and the alarm becomes unmatched the alarm will not occur unless new condition is met. Therefore, take note of this when using the flag.

8.2.5. CLKOUT frequency selection and timer registers

| Address | Function | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0D | CLKOUT frequency | FE | × | × | × | × | × | FD1 | FD0 |
| 0E | Timer control | TE | × | × | × | × | × | TD1 | TD0 |
| 0F | Timer | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |

• Frequency output

| Output frequency | FD1 | FD0 |
|---|---|---|
| 32768 Hz | 0 | 0 |
| 1024 Hz | 0 | 1 |
| 32 Hz | 1 | 0 |
| 1 Hz | 1 | 1 |

∗ At the above setting, the output frequency of the CLKOUT pin can be selected.
Output is possible when the FE of MSB of the D register is 1. (When it stops, the CLKOUT pin goes to LOW.)
These output is controlled by CLKOE pin. When CLKOE input is LOW, CLKOUT output is inhibited.

• Timer control

| Timer source clock | TD1 | TD0 |
|---|---|---|
| 4096 Hz | 0 | 0 |
| 64 Hz | 0 | 1 |
| 1 second | 1 | 0 |
| 1 minute | 1 | 1 |

∗ At the above setting, the count down rate of the timer can be selected.
When the TE of MSB of the E register is 1, the timer count down starts, and stops when it becomes 0.
The F register data counts down at the set frequency and when it becomes zero TF is set.
When the F register is read, the data during count down is read out.

• Timer register

It sets the initial value of the timer's count down. The format is binary.

## 8.3. Access procedure

### 8.3.1. Characteristic of the $I^2C$-BUS

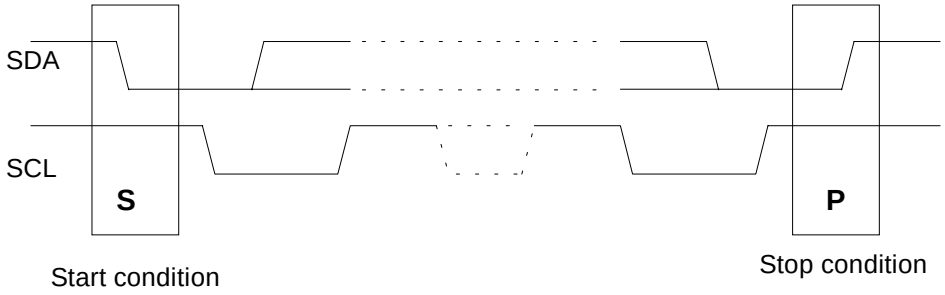
$I^2C$-BUS is a bi-directional interface that uses two (2) lines. This interface has two signal lines, which are SDA (data line) and SCL (clock line). Both of these lines are connected to the $V_{DD}$ line via the pull-up registers. All ports must be open drain or open collector on the $I^2C$-BUS in order to be able to connect multiple devices on this bus using the AND-connection.

### 8.3.2. Bit transfer

The bit data transfer is executed for one bit on each one clock pulse of SCL line. When the device transmits the data, the data change should be executed while SCL line is at LOW. When the device receives the data, the data should be taken in while SCL is at HIGH.

### 8.3.3. Start condition and stop condition

When $I^2C$-BUS is not interfacing, the two control lines keep at HIGH. When SDA changes from HIGH to LOW, this is defined as a start condition. After that, actual data transfer is executed. When SCL is at HIGH and when SDA changes from LOW to HIGH, this is defined as a stop condition.

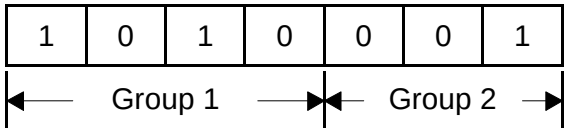



### 8.3.4. Slave address

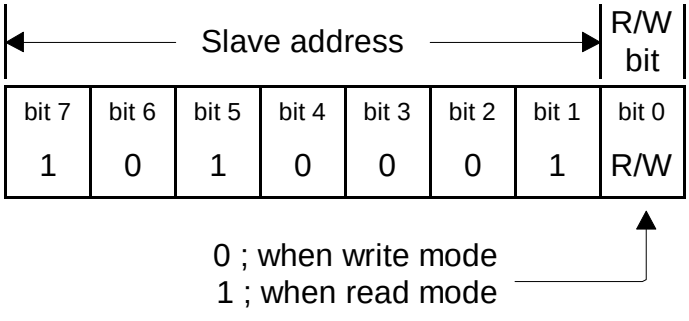
The $I^2C$-BUS devices do not have any chip select pins with the usual logic devices. All $I^2C$-BUS devices have a fixed unique device number for each device built into them. The chip selection on the $I^2C$-BUS is executed when the communication starts and this device number is sent from $I^2C$-BUS as a slave address. The receiving device responds to the communication only if it matches the slave address.

The slave address is a 7-bit data which is made of a 4-bit fixed data (group 1) and 3-bits data (group 2). On the RTC-8564, the data in group 1 is 1010 and in group 2 is 001.

*1) RTC-8564 slave address

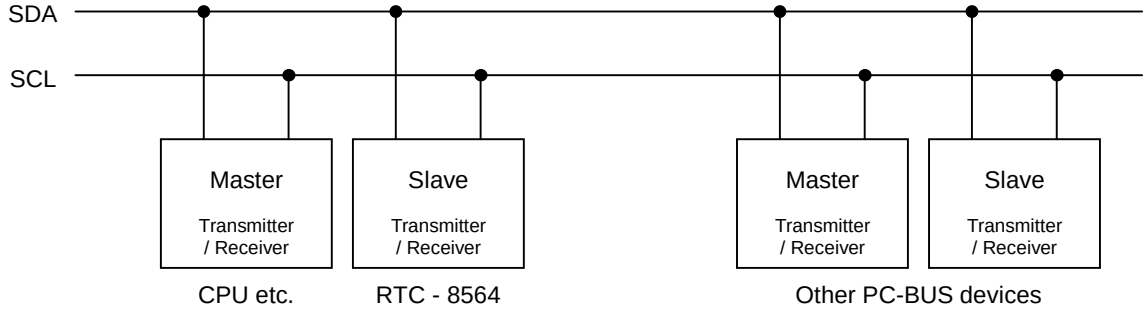



*2) During the actual data transmission, the transmitted data contains both the slave address and the 8-bit data with the added R/W (read/write) bit.



8.3.5. System structure

A master is defined a device that controls interfacing of messages, and a slave is defined as a device which is controlled by the master. A transmitter is defined as a device transmitting messages,and a receiver is defined as the one receiving messages. In the case of the RTC-8564, controllers such as CPU are masters and the RTC-8564 is a slave. Each device can be transmitter and receiver.




8.3.6. Acknowledge

There is no limit to the byte size of data transmitted between the start and stop conditions. For each byte during interfacing, the receiver (receiving end) generates an acknowledge bit to the transmitter (sending end) to confirm that it has received the data. Because the acknowledge bit is LOW active, the transmitter sets the SDA line to HIGH, and sends out a clock pulse for the acknowledge bit. If the receiver can correctly receive the 8-bit data from the transmitter, it will set the SDA line to LOW when the clock for the last bit is finished. Because the $I^2C$-BUS lines are pulled-up, the SDA line of transmitter also turns to LOW. At this moment, the transmitter checks that the acknowledge has returned, and then continues to send out the next data. When the clock pulse for the acknowledge bit is finished, the receiver turns the SDA line to HIGH (release) and prepares to receive the next data.
When a master device is acting as a transmitter and acknowledge is confirmed from the receiver, if the next data is not sent/received but the stop condition is generated, it is possible to terminate the communication normally. When a master device is acting as a receiver and acknowledge bit is sent out as "1", it is possible to terminate the communication normally if the stop condition is generated.

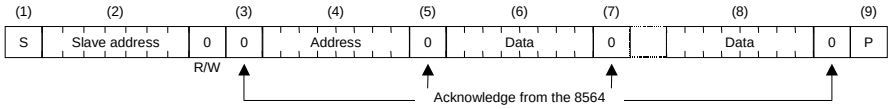
8.3.7. $I^2C$-BUS protocol

The following section describes the communications procedure where the master is CPU and the slave is the RTC-8564.

(1) Procedure for write at specified address

The RTC-8564 has an auto increment function of address. After the initial address is set, if only data continues to be sent, the receiving address on the 8564 is incremented by 1 byte. The procedure as follows:

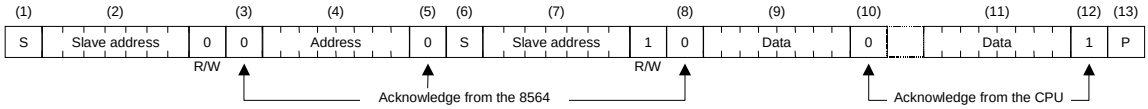
(1) The CPU sends out a start condition.
(2) The CPU sends out the slave address of the 8564 and the R/W bit, in write mode.
(3) Confirm acknowledge from the 8564.
(4) The CPU sends out the write address to the 8564.
(5) Confirm acknowledge from the 8564.
(6) The CPU sends out the data for write to the address specified in step (4).
(7) Confirm acknowledge from the 8564.
(8) If necessary repeat steps (6) and (7). The address will be automatically incremented internally on the 8564.
(9) The CPU sends out the stop condition.




(2) Procedure for read at specified address

According to the write mode, after the address to read is written, the read mode is set and the actual data read. The procedure as follows:

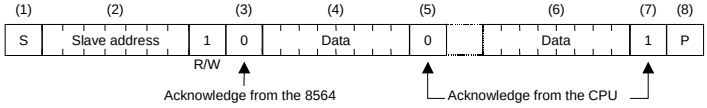
(1) The CPU sends out a start condition.
(2) The CPU sends out the slave address of the 8564 and the R/W bit, in write mode.
(3) Confirm acknowledge from the 8564.
(4) The CPU sends out the address read out from the 8564.
(5) Confirm acknowledge from the 8564.
(6) The CPU sends out the start condition (stop condition is not sent.)
(7) The CPU sends out the slave address of the 8564 and the R/W bit, in read mode.
(8) Confirm acknowledge from the 8564.(From here on, the CPU acts as a receiver and the 8564 as a transmitter.)
(9) Data at the address specified in step (4) is sent out from the 8564.
(10) The CPU sends out acknowledge to the 8564.
(11) If necessary repeat steps (9) and (10). The read address will be automatically incremented internally on the 8564.
(12) The CPU sends out the stop condition.



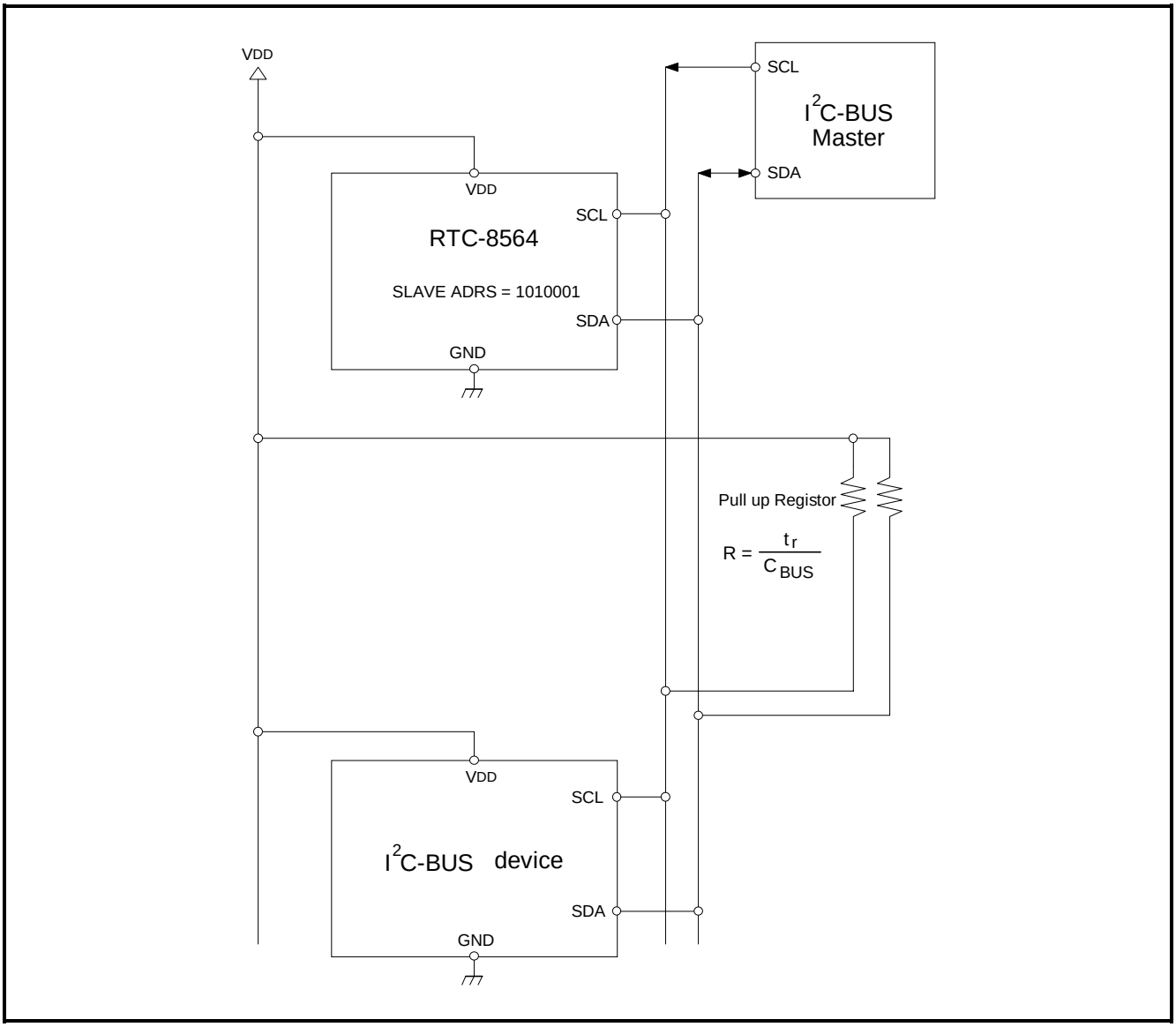

(3) Read procedure without specified address

Immediately after the read mode is set up, data can be read. In this case, the address is the address when the previous access ended, plus 1. The procedure is as follows:

(1) The CPU sends out a start condition.
(2) The CPU sends out the slave address of the 8564 and the R/W bit, in read mode.
(3) Confirm acknowledge from the 8564.(From here on, the CPU acts as a receiver and the 8564 as a transmitter.)
(4) Data at the last address in the previous access plus 1 is sent out from the 8564.
(5) The CPU sends out acknowledge to the 8564.
(6) If necessary repeat steps (4) and (5). The read address will be automatically incremented internally on the 8564.
(7) The CPU sends out acknowledge of "1".
(8) The CPU sends out the stop condition.



8.4. Typical connection to micro computers

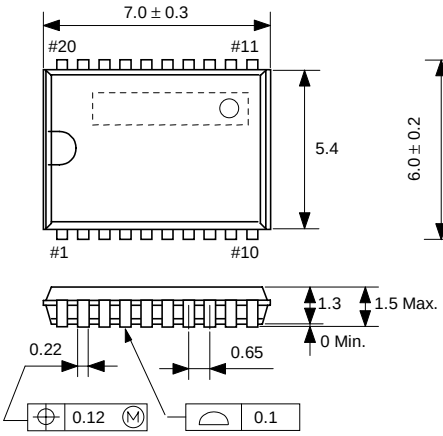


# 9. External dimensions / Marking layout

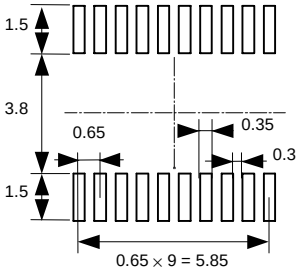
## 9.1. External dimensions

### RTC - 8564 JE ( VSOJ-20pin )

• External dimensions




• Recommended soldering pattern

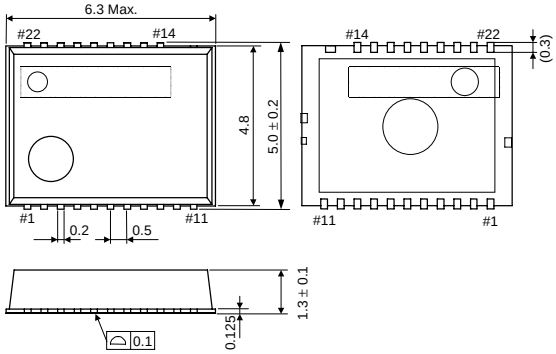



Unit : mm

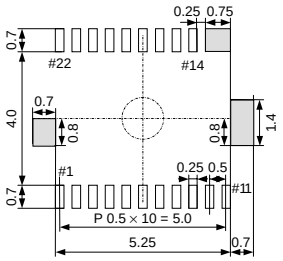
∗ The cylinder of the crystal oscillator can be seen in this area ( back and front ), but it has no affect on the performance of the device.

### RTC - 8564 NB ( SON-22pin )

• External dimensions




• Soldering pattern



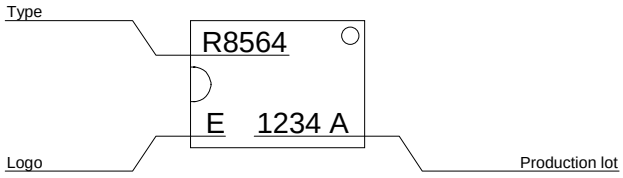

Unit : mm

∗1) The cylinder of the crystal oscillator can be seen in this area ( back and front ), but it has no affect on the performance of the device.

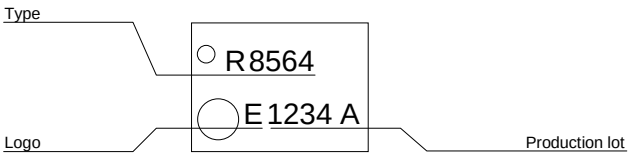
∗2) In this area, At a parts side of electronic base, you must not do layout any signal line.

## 9.2. Marking layout

### RTC - 8564 JE ( VSOJ-20pin )



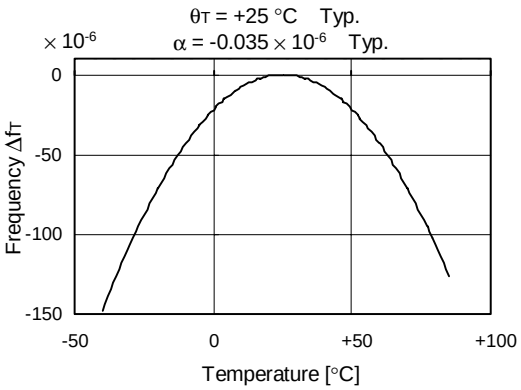

### RTC - 8564 NB ( SON-22pin )



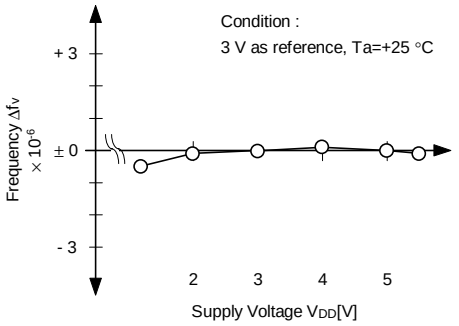

∗ Contents displayed indicate the general markings and display, but are not the standards for the fonts, sizes and positioning.

# 10. Reference data

(1)Example of frequency and temperature characteristics




(2) Example of frequency and voltage characteristics




[Finding the frequency stability]

1. Frequency and temperature characteristics can be approximated using the following equations.

$\Delta f_T = \alpha ( \theta_T - \theta_X )^2$

| | | |
|---|---|---|
| $\Delta f_T$ | | : Frequency deviation in any temperature |
| $\alpha$ | ( $1 / °C^2$ ) | : Coefficient of secondary temperature ( ( $-0.035 \pm 0.005$ ) $\times 10^{-6} / °C^2$ ) |
| $\theta_T$ | ( °C ) | : Ultimate temperature (+25±5 °C) |
| $\theta_X$ | ( °C ) | : Any temperature |

2. To determine overall clock accuracy, add the frequency precision and voltage characteristics.

$\Delta f/f = \Delta f/fo + \Delta f_T + \Delta fv$

| | |
|---|---|
| $\Delta f/f$ | : Clock accuracy (stable frequency) in any temperature and voltage. |
| $\Delta f/fo$ | : Frequency precision |
| $\Delta f_T$ | : Frequency deviation in any temperature. |
| $\Delta fv$ | : Frequency deviation in any voltage. |

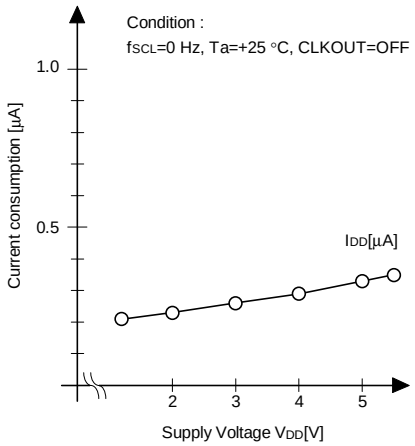
3. How to find the date difference

Date Difference = $\Delta f/f \times 86400$(Sec)

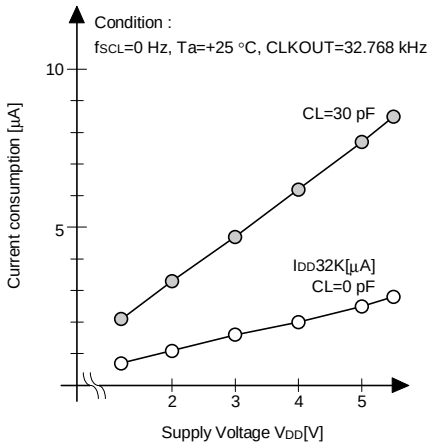
* For example: $\Delta f/f = 11.574 \times 10^{-6}$ is an error of approximately 1 second/day.

(3) Current and voltage consumption characteristics

(3-1) Current consumption when non-accessed (i) when CLKOUT=OFF




(3-2) Current consumption when non-accessed (ii) when CLKOUT=32.768kHz



# 11. Application notes

## 11.1. Notes on handling

This module uses a C-MOS IC to realize low power consumption. Carefully note the following cautions when handling.

(1) Static electricity

While this module has built-in circuitry designed to protect it against electrostatic discharge, the chip could still be damaged by a large discharge of static electricity. Containers used for packing and transport should be constructed of conductive materials. In addition, only soldering irons, measurement circuits, and other such devices which do not leak high voltage should be used with this module, which should also be grounded when such devices are being used.

(2) Noise

If a signal with excessive external noise is applied to the power supply or input pins, the device may malfunction or "latch up." In order to ensure stable operation, connect a filter capacitor (preferably ceramic) of greater that 0.1F as close as possible to the power supply pins (between $V_{DD}$ and GNDs). Also, avoid placing any device that generates high level of electronic noise near this module.

* Do not connect signal lines to the shaded area in the figure shown in Fig. 1 and, if possible, embed this area in a GND land.

(3) Voltage levels of input pins

When the input pins are at the mid-level, this will cause increased current consumption and a reduced noise margin, and can impair the functioning of the device. Therefore, try as much as possible to apply the voltage level close to $V_{DD}$ or GND.

(4) Handling of unused pins

Since the input impedance of the input pins is extremely high, operating the device with these pins in the open circuit state can lead to unstable voltage level and malfunctions due to noise. Therefore, pull-up or pull-down resistors should be provided for all unused input pins.

## 11.2. Notes on packaging

(1) Soldering heat resistance

If the temperature within the package exceeds +260, the characteristics of the crystal oscillator will be degraded and it may be damaged. The reflow conditions within our reflow profile is recommended.
Therefore, always check the mounting temperature and time before mounting this device.
Also, check again if the mounting conditions are later changed.

* See Fig. 2 profile for our evaluation of Soldering heat resistance for reference.

(2) Mounting equipment

While this module can be used with general-purpose mounting equipment, the internal crystal oscillator may be damaged in some circumstances, depending on the equipment and conditions. Therefore, be sure to check this. In addition, if the mounting conditions are later changed, the same check should be performed again.

(3) Ultrasonic cleaning

Depending on the usage conditions, there is a possibility that the crystal oscillator will be damaged by resonance during ultrasonic cleaning. Since the conditions under which ultrasonic cleaning is carried out (the type of cleaner, power level, time, state of the inside of the cleaning vessel, etc.) vary widely, this device is not warranted against damage during ultrasonic cleaning.

(4) Mounting orientation

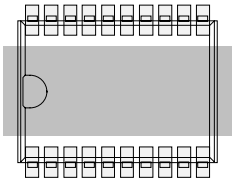
This device can be damaged if it is mounted in the wrong orientation. Always confirm the orientation of the device before mounting.

(5) Leakage between pins

Leakage between pins may occur if the power is turned on while the device has condensation or dirt on it. Make sure the device is dry and clean before supplying power to it.

Fig. 1: Example GND Pattern

RTC - 8564 JE ( VSOJ-20pin )



RTC - 8564 NB ( SON-22pin )

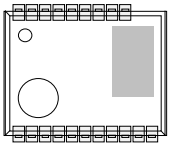
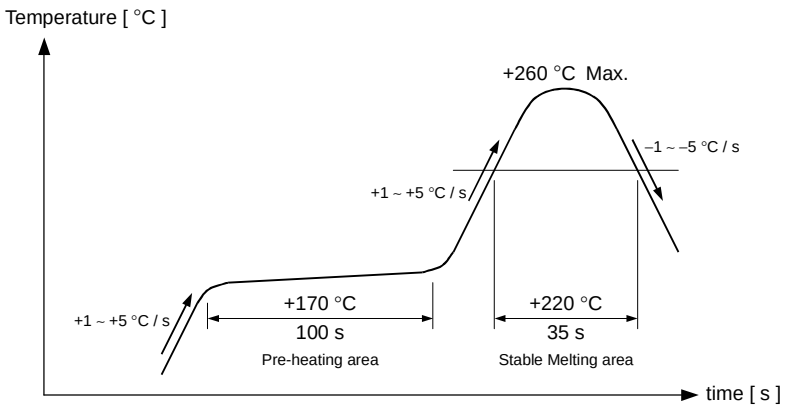


Fig. 2: Reference profile for our evaluation of Soldering heat resistance.



# EPSON
# Application Manual

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